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MICROCOMPUTER MN15G

MN15G0202/0402
LSI User's Manual

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About This Manual

■Organization

In this LSI manual, this LSI functions are presented in the following order : overview, basic CPU functions, interrupt functions, port functions, timer functions, serial functions, and other peripheral hardware functions.

Each section contains overview of function, block diagram, control register, operation, and setting example.

■Manual Configuration

Each section of this manual consists of a title, summary, main text, key information, precautions and warnings, and references.

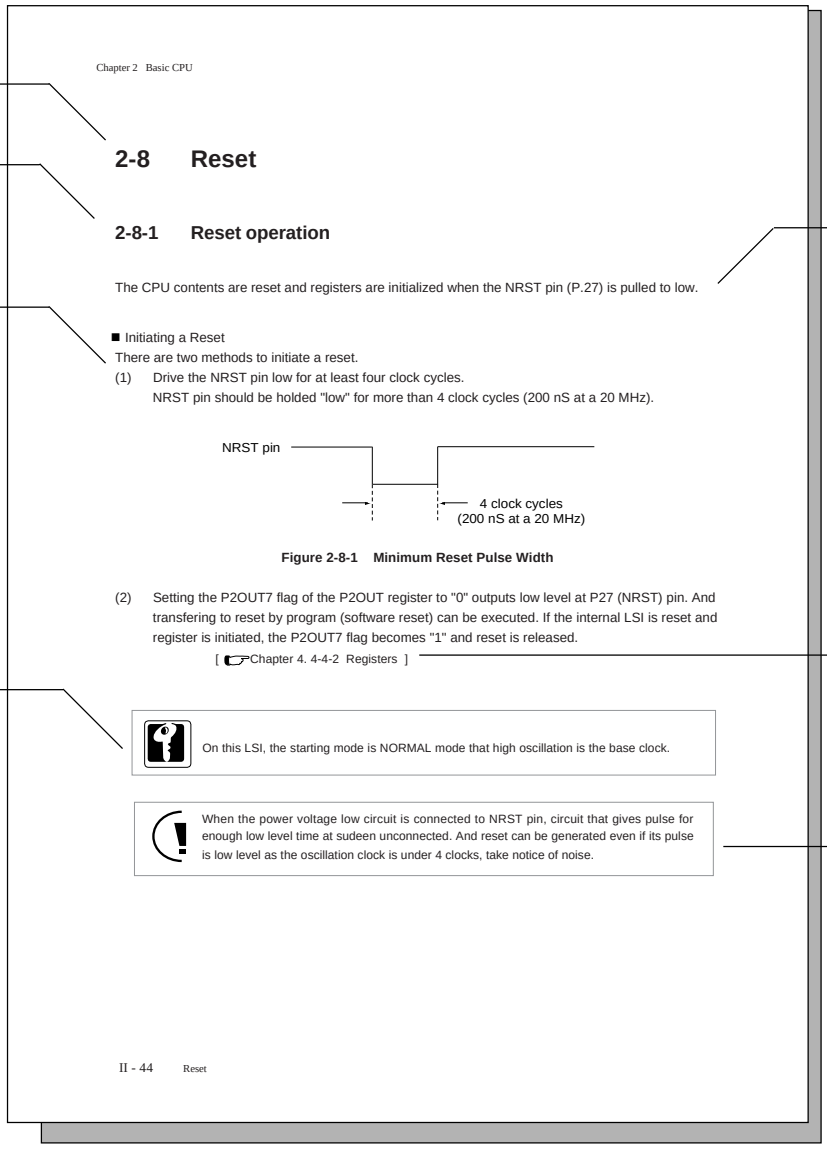
The layout and definition of each section are shown below.

Subtitle

Sub-subtitle
The smallest block in this manual.

Main text

Key information
Important information from the text.



Summary
Introduction to the section.

References
References for the main text.

Precautions and warnings
Precautions are listed in case.
Be sure to read these of lost functionality or damage.

■Finding Desired Information

This manual provides three methods for finding desired information quickly and easily.

(1) Consult the index at the front of the manual to locate the beginning of each section.
(2) Consult the table of contents at the front of the manual to locate desired titles.
(3) Chapter names are located at the top outer corner of each page, and section titles are located at the bottom outer corner of each page.

■Related Manuals

Note that the following related documents are available.

"MN1500 Series Instruction Manual"
<Describes the instruction set.>
"MN1500 Series Cross-assembler User's Manual"
<Describes the assembler syntax and notation.>
"MN1500 Series Source Code Debugger User's Manual"
<Describes the use of source code debugger.>
"MN1500 Series PanaX Series Installation Manual"
<Describes the installation of cross-assembler and source code debugger and the procedure for bringing up the in-circuit emulator.>

■Where to Send Inquires

We welcome your questions, comments, and suggestions. Please contact the semiconductor design center closest to you. See the last page of this manual for a list of addresses and telephone numbers.

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Chapter 1 Overview

Chapter 2 Basic CPU

Chapter 3 Ports

Chapter 4 Interrupts

Chapter 5 Timers

Chapter 6 A/D Converter

Chapter 7 AC Zero-Cross Detection

Chapter 8 Watchdog Timer

Chapter 9 Automatic Reset

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Chapter 1 Overview

1-1 Overview

This LSI is 4-bit single-chip microcomputer. The MN15G0202 has an internal 2 KB of ROM and 128 nibble of RAM and the MN15G0402 has an internal 4 KB of ROM and 128 nibble of RAM. Peripheral functions include 2 sets of 8-bit timer counters (They can be used as 16-bit counter on cascade connection.), 10-bit A/D converter, AC zero-cross detection circuit, buzzer output circuit and LED driver pins.

1-1-1 Product Summary

This manual describes the following models of the MN15GXX02 series. These products have identical functions.

Table 1-1-1 Product Summary

Model	ROM Size	RAM Size	Classification
MN15G0202	2 KB	128 nibble	Mask ROM version
MN15G0402	4 KB	128 nibble	Mask ROM version
MN15GP0402SJ	4 KB	128 nibble	EPROM version

Table 1-1-2 Differences in Models

Parameter		MN15G0202	MN15G0402	MN15GP0402SJ
Power supply voltage		2.0 V to 5.5 V	2.0 V to 5.5 V	2.3 V to 5.5 V
Ambient operating temperature		-40 °C to +85 °C	-40 °C to +85 °C	-20 °C to +70 °C
Mask option	Automatic reset circuit	1 : unused 2 : Automatic reset 1 3 : Automatic reset 2	1 : unused 2 : Automatic reset 1 3 : Automatic reset 2	1 : unused

For mask option, refer to 1-8 Option.

1-2 Hardware Functions

Table 1-2-1 Basic Specification

Model	MN15G0202	MN15G0402	MN15GP0402
ROM version	Mask ROM version		EPROM version
ROM	2 KB	4KB	4KB
RAM	128 nibble	128 nibble	128 nibble

Package **20SOP**

Machine cycle **When automatic reset is not used :**

0.50 µs / 8 MHz	divided by 4	(3.0 V to 5.5 V)
1.00 µs/ 4 MHz	divided by 4	(2.4 V to 5.5 V)
2.00 µs/ 4 MHz	divided by 8	(2.0 V to 5.5 V)

When automatic reset circuit 1 is used :

0.50 µs / 8 MHz	divided by 4	(V_{RSTL1} to 5.5 V)
1.00 µs/ 4 MHz	divided by 4	(V_{RSTL1} to 5.5 V)
2.00 µs/ 4 MHz	divided by 8	(V_{RSTL1} to 5.5 V)

When automatic reset circuit 2 is used :

2.00 µs / 4 MHz	divided by 8	(V_{RSTL2} to 5.5 V)

Back up mode HALT mode
STOP mode

Ambient operating temperature
-40 °C to +85 °C
(-20 °C to +70 °C for MN15GP0402SJ)

Interrupts **3 levels**
- Interrupt 1 (IRQ1)
- Interrupt 2 (IRQ2)
- Interrupt 3 (IRQ3)

Timers / Counters

3 timers

Timer 2 (8-Bit timer for general use)

- Timer pulse output, PWM output, Remote control carrier output
- Clock source
  fsys/2, fsys/8, fsys/32, fsys/128, fosc, fosc/4, fosc/16, fosc/64

Timer 3 (8-Bit timer for general use)

- Timer pulse output, High precision PWM output, Remote control carrier output, 16-Bit cascade connection function (connected to timer 2)
- Clock source
  fsys/2, fosc, fosc/2^{6}, fosc/2^{14}

Watchdog timer

A/D converter 10 bits X 4 channels

Buzzer output Output frequency can be selected from fosc/1024, fosc/2048, fosc/4096.

PWM output

Remote control output Duty cycle of 1/2, or 1/3.

ACZ input 1 set

Mask option Automatic reset is available.

Port

General I/O ports	15 ports (11 ports can be used for other functions)
- Buzzer output	1 ports (for timer output and key input, too)
- Timer output	1 ports (for buzzer output and key input, too)
- NSYNC output	1 ports (for key input, too)
- ACZ input	1 ports (for NIRQ input and key input, too)
- NIRQ input	1 ports (for ACZ input and key input, too)
- A/D converter input	4 ports
- Key input	3 ports (for NSYNC output, NIRQ input, ACZ input, timer output and buzzer output, too)
- PWM output	4 ports

EPROM version MN15GP0402SJ

Emulator PX-ICE1500+PX-PRB15G0402

Process CMOS

1-3 Block Diagram

1-3-1 Overview

Table 1-3-1 Functions on Blocks

Name	Block	Description
CPU(MN150G)	Instruction execution controller	Controls CPU block operations in response to the result decoded by the instruction decoder and interrupt requests.
ROM	Memory data	Read Only Memory can be used as an area where instructions that CPU executes are stored.
RAM		Random Access Memory can be used as an data area where data that are needed on program execution are stored and as the stack area.
Timer 2, 3 Buzzer output	Timer controller	Used as timer operation, timer pulse output, PWM output, cascade connection, remote control carrier output, buzzer output.
A/D converter	A/D controller	Includes a set of A/D converter with 10-bits resolution. Analog input is switched channel 0 to 3(AD0 to AD3) by software.
External interrupt	Interrupt controller	Controls interrupt by interrupt request flag (IF) and interrupt enable flag (IE).
Port 0 Port 1 Port 2 Port 3	I/O controller	Port 0, port 1, port 2, port 3 are I/O port.
Clock generator	Clock generator	Connect resonator to OSC1, OSC2 to generate systemclock.
Watchdog timer	Error detector	Counts watchdog timer. When counter is overflow, output "L" from NRST pin and reset.
Automatic reset	Low voltage detector	When low voltage is detected, output "L" from NRST pin and reset.

1-3-2 Block Diagram

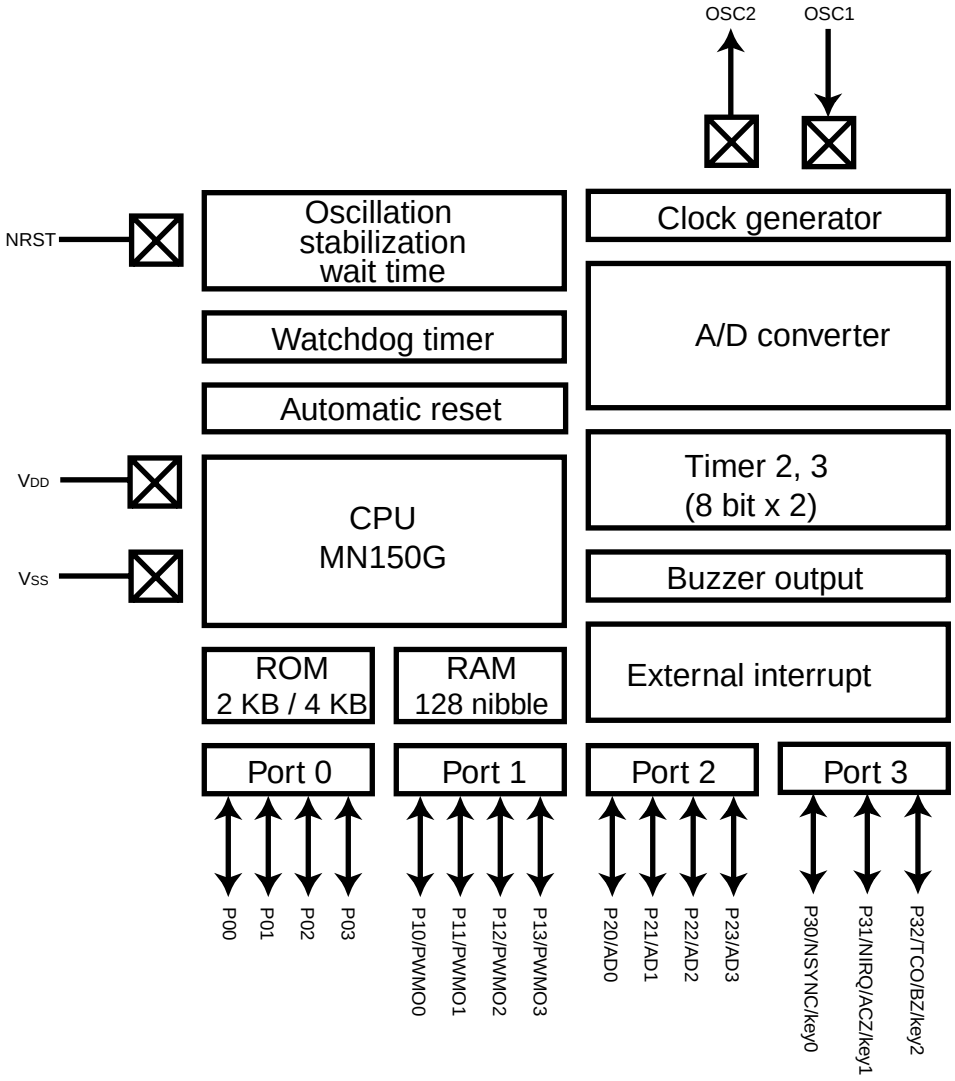


Figure 1-3-1 Block Function Diagram

1-4 Pin Description

1-4-1 Pin Configuration

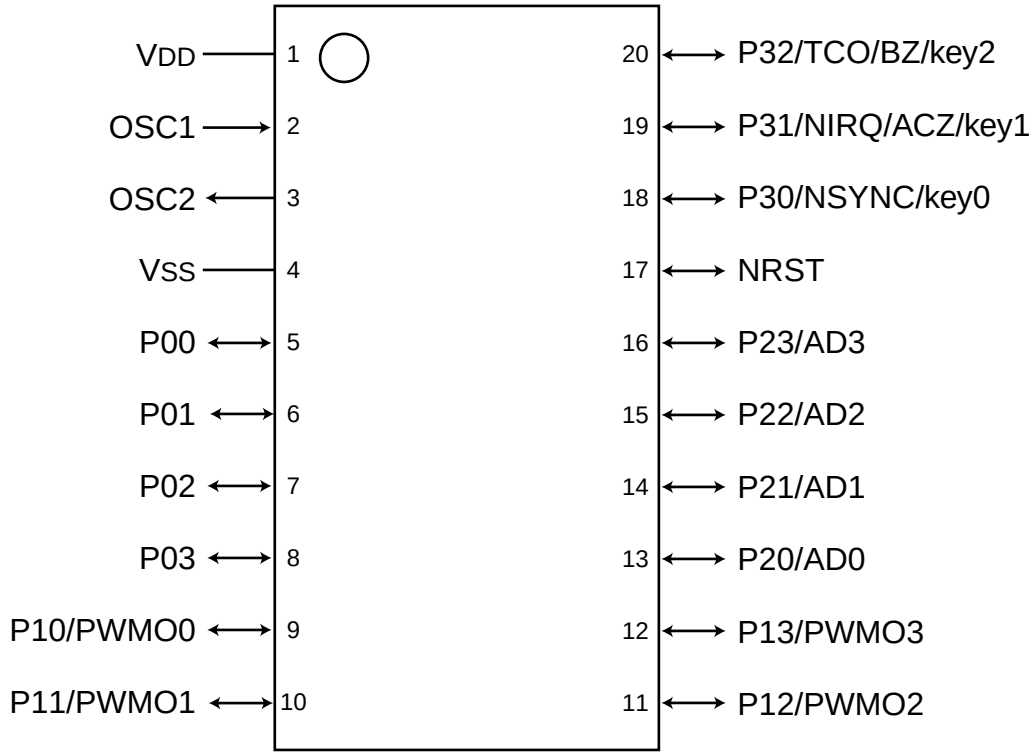


Figure 1-4-1 Pin Configuration (20SOP : Top view)

1-4-2 Pin Functions

Table 1-4-1 Pin Function Summary (1/3)

Name	Pin No.	I/O	Dual Function	Function	Description
VSS VDD	4 1	-		Power supply pin	Apply 2.0 V to 5.5 V to VDD and 0 V to VSS.
OSC1 OSC2	2 3	Input Output		Clock input pin Clock output pin	Connect these oscillation pins to oscillators for clock operation. Feed back resistor is buit-in. If the clock is an external input, connect it to OSC1 and leave OSC2 open.
NRST	17	I/O		Reset input pin [Schmitt]	Reset by inputting "L" to NRST pin. After reset is cleared, internal reset is cleared after 2^{14} counts of OSC input clock. The output configuration is N-ch open-drain. Reset can be selected by watchdog timer or low voltage detector(*1) by automatic reset circuit. *1 Autoreset circuit is mask option.
P00 P01 P02 P03	5 6 7 8	I/O		I/O port 0	Parallel data I/O port. Each bit can be set individually as either an input or output by the P01DIR register. The output configuration is N-ch open-drain. At reset, the input mode (high impedance output) is selected.
P10 P11 P12 P13	9 10 11 12	I/O	PWMO0 PWMO1 PWMO2 PWMO3	I/O port 1	Parallel data I/O port. Each bit can be set individually as either an input or output by the P01DIR register. The output configuration is CMOS push-pull or N-ch open-drain. Each bit can be switched individually by the P01SC register. At reset, the input mode (high impedance output) is selected. They can be also used for PWM output (PWMO0 to 3).
P20 P21 P22 P23	13 14 15 16	I/O	AD0 AD1 AD2 AD3	I/O port 2	Parallel data I/O port. Each bit can be set individually as either an input or output by the P23DIR register. A pull-up resistor for each bit can be selected individually by the P23PLU register. The output configuration is CMOS push-pull or N-ch open-drain. Each bit can be switched individually by the P23SC register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output). P20 / AD0, P21 / AD1, P22 / AD2 and P23 / AD3 are dual functions.

Table 1-4-2 Pin Function Summary (2/3)

Name	Pin NO.	I/O	Dual Function	Function	Description
P30 P31 P32	18 19 20	I/O	NSYNC key0 NIRQ ACZ key1 TCO BZ key2	I/O port 3 [Schmitt]	Parallel data I/O port. Each bit can be set individually as either an input or output by the P23DIR register. A pull-up resistor for each bit can be selected individually by the P23PLU register. The output configuration is CMOS push-pull or N-ch open-drain. Each bit can be set individually by the P23SC register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output), but P30 outputs system clock during the internal reset. P30 / NSYNC, P31 / NIRQ/ACZ and P32 / TCO/BZ are dual functions. These can be used as key interrupt input.
AD0 AD1 AD2 AD3	13 14 15 16	Input	P20 P21 P22 P23	Analog input pin	Analog input pins for 4 channels. Set pin's direction to input by the P23DIR resister. When not used for analog input, these pins can be used as normal port.
NSYNC	18	Output	P30 key0	Systemclock synchronous output	At internal reset, synchronous signal of system clock is output. At operation, the initial status is port, but NSYNC output / port data output can be selected by the ACZCNT register. These can be used as key interrupt input.
ACZ	18	Input	P31 NIRQ key1	AC zero-cross detection input	AC zero-cross detection circuit input pin. AC zero-cross detection circuit is connected to ACZ interrupt input and P31 input circuit. P31 ACZ input / port input can be selected by the ACZCNT register. These can be used as key interrupt input.
BZ	20	Output	P32 TCO key2	Buzzer output	Buzzer output pin. Buzzer output / port data output can be selected by the BZCTR register. When not used for buzzer output, this can be used as normal port. This can be used as Key interrupt input.
NIRQ	19	Input	P31 ACZ key1	Interrupt input	Interrupt 1 (IRQ1) input pin. When not used for interrupt input, this can be used as normal port. This can be used as key interrupt input.
TCO	20	Output	P32 BZ key2	Timer output	Timer output pins. Timer output / port data output can be selected by the TCOCNT register. When not used for timer output, this pin can be used as normal port. This can be used as key interrupt input.

Table 1-4-3 Pin Function Summary (3/3)

Name	Pin NO.	I/O	Dual Function	Function	Description
key0 key1 key2	18 19 20	Input	P30 NSYNC P31 NIRQ ACZ P32 TCO BZ	Key interrupt input	Key interrupt input. Each bit can be set individually as either an enable or disable by the KEYCNT register. When not used for key interrupt input, these pins can be used as normal port.
PWMO0 PWMO1 PWMO2 PWMO3	9 10 11 12	Output	P10 P11 P12 P13	PWM output	PWM output pins. Each bit can be set individually PWM output as either an enable or disable by the BZCTR register. When PWM output is enabled, the conjunction of the timer output selected by the MODCNT register and the port output latch data is output.

1-5 Special Function Registers

1-5-1 Register Map

This special function registers of this LSI are located as shown below.

Table 1-5-1 Register Map

Page 0

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 x	PORT0		PORT1		PORT2		PORT3									
1 x	P01DIR				P23DIR											
2 x			P23PLU						P01SC		P23SC					
3 x	CPUM		IRQM		IRQC0		IRQC1		KEYCNT		ACZCNT					
4 x					TM2BC		TM3BC						TM2MD		TM3MD	
5 x					TM2OC		TM3OC								MODCNT	
6 x											TCOCNT		BZCTR		WDCTR	
7 x	ADBUF0		ADBUF1		ADCTR0											
8 x																
9 x																
A x																
B x																
C x																
D x																
E x																
F x																

Note : Access to x'000' to x'00F' is by 4-bit (I/O instruction on each port) and 8-bit.
Access to x'010' to x'07F' is by only 8-bit.

1-5-2 Special Function Registers

Address	Register	R/W	Function	Page
x'000'	PORT01	R/W	Port 0, port 1 data register	Ⅲ - 9
x'002'	PORT23	R/W	Port 2, port 3 data register	Ⅲ - 13
x'010'	P01DIR	R/W	Port 0, port 1 direction control register	Ⅲ - 9
x'012'	P23DIR	R/W	Port 2, port 3 direction control register	Ⅲ - 13
x'022'	P23PLU	R/W	Port 2, port 3 pull-up resistor control register	Ⅲ - 13
x'028'	P01SC	R/W	Port 1 output structure control register	Ⅲ - 9
x'02A'	P23SC	R/W	Port 2, port 3 output structure control register	Ⅲ - 14
x'030'	CPUM	R/W	CPU mode register	Ⅱ - 15
x'032'	IRQM	W	IRQ mode register	Ⅳ - 16
x'034'	IRQC0	R/W	Interrupt 0 control register	Ⅳ - 16
x'036'	IRQC1	R/W	Interrupt 1 control register	Ⅳ - 17
x'038'	KEYCNT	R/W	Key interrupt 1 control register	Ⅳ - 17
x'03A'	ACZCNT	R/W	ACZ control register	Ⅶ - 5
x'044'	TM2BC	R	Timer 2 binary counter	Ⅴ - 10
x'046'	TM3BC	R	Timer 3 binary counter	Ⅴ - 10
x'04C'	TM2MD	R/W	Timer 2 mode register	Ⅴ - 11
x'04E'	TM3MD	R/W	Timer 3 mode register	Ⅴ - 12
x'054'	TM2OC	R/W	Timer 2 compare register	Ⅴ - 9
x'056'	TM3OC	R/W	Timer 3 compare register	Ⅴ - 9
x'05E'	MODCNT	R/W	Timer mode control register	Ⅴ - 12
x'06A'	TCOCNT	R/W	Timer output control register	Ⅴ - 13
x'06C'	BZCTR	R/W	Buzzer output control register	Ⅴ - 14
x'06E'	WDCTR	W	Watchdog timer control register	Ⅷ - 4
x'070'	ADBUF0	R	A/D converter data storage buffer 0	Ⅵ - 6
x'072'	ADBUF1	R	A/D converter data storage buffer 1	Ⅵ - 6
x'074'	ADCTR0	R/W	A/D control register	Ⅵ - 5

R/W : Readable / Writable

R : Readable only

W : Writable only

1-6 Electrical Characteristics

This LSI user's manual describes the standard specification. Please ask our sales offices for its own product specifications.

Contents \ Model	MN15G0202, MN15G0402
Structure	CMOS integrated circuit
Application	General purpose
Function	CMOS, 4-bit, single-chip microcontroller

1-6-1 Absolute Maximum Ratings *2 *3

V_{SS} = 0 V

	Parameter		Symbol	Rating	Unit
1	Power supply voltage		V_{DD}	-0.3 to +7.0	V
2	Input clamp current (ACZ)		I_C	-0.5 to +0.5	mA
3	I/O pin voltage		V_{IO}	-0.3 to V_{DD}+0.3 (except ACZ)	V
4	Peak output current	P0	$I_{OL(peak)}$	40	mA
5		Other than P0	$I_{OL(peak)}$	20	
6		all	$I_{OH(peak)}$	-10	
7	Average output current *1	P0	$I_{OL(avg)}$	15	
8		Other than P0	$I_{OL(avg)}$	10	
9		all	$I_{OH(avg)}$	-2	
10	Total output current *1	P0	I_{TOL1}	60-I_{TOL2}	
11		Other than P0	I_{TOL2}	20	
12		P0	I_{TOH1}	60-I_{TOH2}	
13		Other than P0	I_{TOH2}	20	
14	Power dissipation		P_D	180(Ta=85 °C)	mW
15	Ambient operating temperature		T_{opr}	-40 to +85	°C
16	Storage temperature		T_{stg}	-55 to +125	°C

*1 Applied to any 100-ms period.

*2 Connect at least one bypass capacitor of 0.1µF or larger between the power supply pin and the ground, near the LSI, for latch-up prevention.

*3 The absolute maximum ratings are the limit values beyond which the LSI may be damaged and proper operation is not assured. They do not assure operation.

1-6-2 Operating Conditions

Ta = -40 °C to +85 °C V_{DD} = 2.0 V to 5.5 V($V_{RSTL1,2}$ to 5.5 V) V_{SS} = 0 V

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply voltage							
1	Power supply voltage	V_{DD1}	fosc≤8 MHz(divided by 4) No automatic reset	3.0	-	5.5	V
2		V_{DD2}	fosc≤4 MHz(divided by 4) No automatic reset	2.4	-	5.5	
3		V_{DD3}	fosc≤4 MHz(divided by 8) No automatic reset	2.0	-	5.5	
4		V_{DD4} *1	fosc≤8 MHz(divided by 4) fosc≤4 MHz(divided by 4) Automatic reset	V_{RSTL1}	-	5.5	
5		V_{DD5}	fosc≤4 MHz(divided by 8) Automatic reset	V_{RSTL1} V_{RSTL2}	-	5.5	
*1 Automatic reset circuit 2 cannot be selected in mask option. Note : V_{RSTL1} and V_{RSTL2} is applied when automatic reset circuit is selected in mask option. They are voltage to activate reset by detecting power supply voltage.							
Automatic reset circuit 1							
6	Power supply detection level	V_{RSTH1}	figure 1-6-1.	-	3.90	4.40	V
7		V_{RSTL1}		3.20	3.70	-	
8	Hysteresis width	Vh		0.05	0.20	-	
9	Power supply voltage change	Δt/Δv		1.00	-	-	ms/V
Automatic reset circuit 2							
10	Power supply detection level	V_{RSTH2}	figure 1-6-1.	-	2.20	2.40	V
11		V_{RSTL2}		1.80	2.05	-	
12	Hysteresis width	Vh		0.05	0.15	-	
13	Power supply voltage change	Δt/Δv		1.00	-	-	ms/V

Ta = -40 °C to +85 °C V_{DD} = 2.0 V to 5.5 V($V_{RSTL1,2}$ to 5.5 V) V_{SS} = 0 V

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Operation speed							
14	Instruction execution time	t_{c1}	V_{DD}=3.0 V to 5.5 V (): At automatic reset	0.5	-	16	µs
15		t_{c2}	V_{DD}=2.4 V(V_{RSTL1}) to 5.5 V (): At automatic reset	1.0	-	16	
16		t_{c3}	V_{DD}=2.0 V($V_{RSTL1,2}$) to 5.5 V High oscillation (): At automatic reset	2.0	-	16	

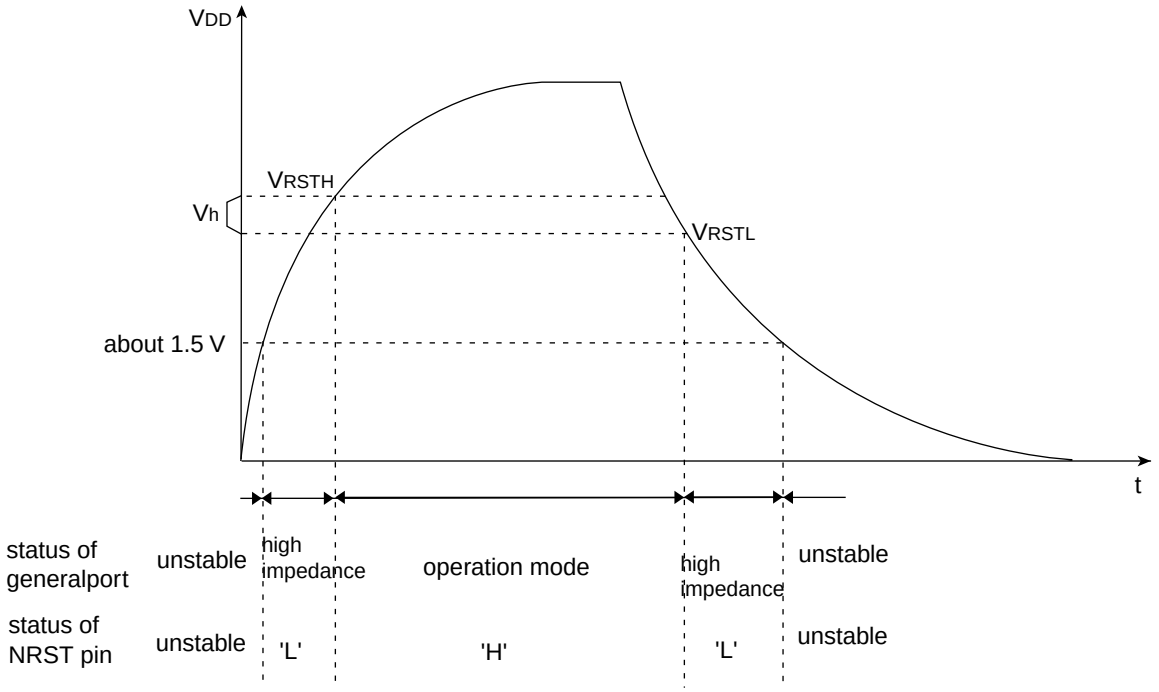


Figure 1-6-1 Automatic Reset Voltage

Ta = -40 °C to +85 °C V_{DD} = 2.0 V to 5.5 V($V_{RSTL1,2}$ to 5.5 V) V_{SS} = 0 V

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Oscillation (High oscillation)							
17	Oscillation frequency	f_{xtal1}	V_{DD}=2.0 V to 5.5 V V_{DD}=$V_{RSTL1, 2}$ to 5.5 V *1 figure 1-6-2.	0.5	-	8.0	MHz
18	External capacitors	C_{11}		-	30.0	-	pF
19		C_{12}		-	30.0	-	
20	Internal feedback resistor	R_{F1}		-	500.0	-	kΩ

*1 When automatic reset is available

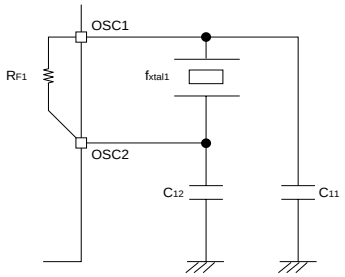


Figure 1-6-2 Oscillation

Connect the external capacitor suits the used pin. When crystal oscillator or ceramic oscillator is used , frequency is changed depending on the condenser rate. Therefore, please consult the manufacturer the external capacitors suits the used pin.

Ta = -40 °C to +85 °C V_{DD} = 2.0 V to 5.5 V($V_{RSTL1,2}$ to 5.5 V) V_{SS} = 0 V

Parameter		Symbol	Conditions	Rating			Unit
External clock input OSC 1(OSC2 is unconnected.)							
21	Clock frequency	f_{osc1}		0.5	-	8.0	MHz
22	High level pulse width	t_{wh1}	figure 1-6-3. *1	56	-	-	ns
23	Low level pulse width	t_{wl1}		56	-	-	
24	Rise time	t_{wr1}	figure 1-6-3.	-	-	20	
25	Fall time	t_{wf1}		-	-	20	

*1 The clock duty cycle should be 45 % to 55 %.

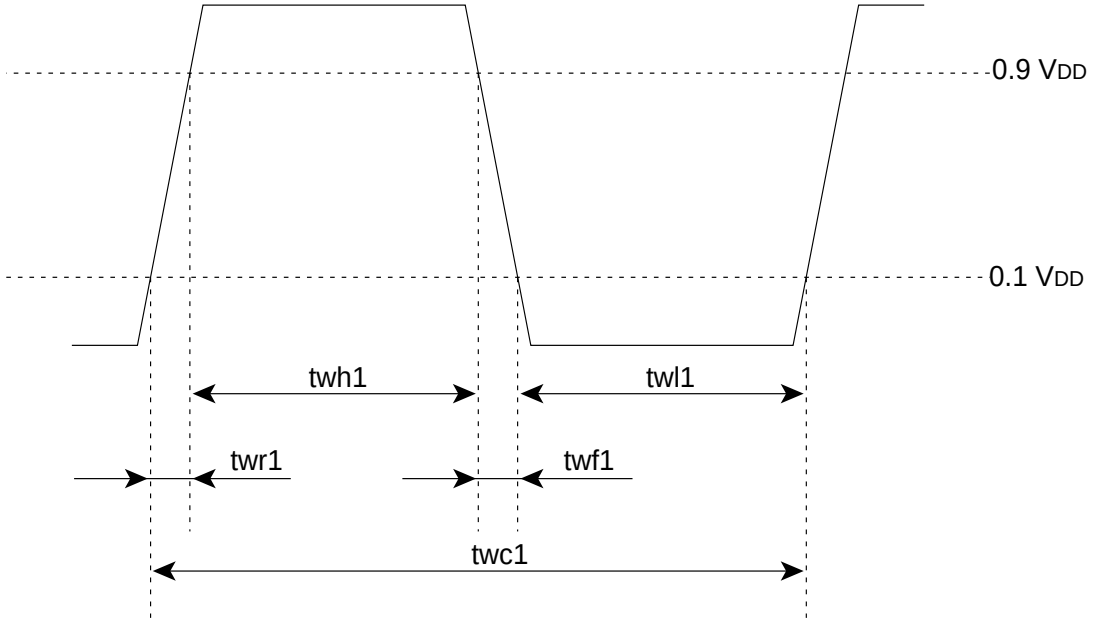


Figure 1-6-3 OSC1 Timing Chart (External clock input)

1-6-3 DC Characteristics

Ta = -40 °C to +85 °C V_{DD} = 2.0 V to 5.5 V($V_{RSTL1,2}$ to 5.5 V) V_{SS} = 0 V

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply current *1							
1	Power supply current	I_{DD1}	fosc=8.0 MHz (divided by 8) V_{DD}=5.0 V	-	1.5	3.0	mA
2		I_{DD2}	fosc=4.0 MHz (divided by 8) V_{DD}=5.0 V	-	1.2	2.5	
3	Supply current during HALT mode	I_{DD3}	fosc=4.0 MHz (divided by 8) V_{DD}=5.0 V	-	0.3	0.6	mA
4	Supply current during STOP mode	I_{DD4}	V_{DD}=5 V ACZ=1/2V_{DD} Ta=25 °C	-	3.0	10.0	µA
5		I_{DD5}	V_{DD}=5 V ACZ=1/2V_{DD} Ta = -40 °C to +85 °C	-	-	20.0	
6		I_{DD6}	V_{DD}=5 V Ta=25 °C	-	-	1.0	
7		I_{DD7}	V_{DD}=5 V Ta=-40 °C to +85 °C	-	-	5.0	
8	Automatic reset current consumption *2	I_{DD8}	V_{DD}=5 V	-	4.0	8.0	

*1 Measured under conditions of no load, Ta = 25 °C.

*2 The automatic reset current consumption I_{DD10} indicates the consumption, normally spent in automatic reset circuit, when automatic reset is used in mask option. So, if automatic reset circuit is selected, each rating is added.

- The supply current during operation, I_{DD1}, is measured under the following conditions :
  After reset is released and the oscillation is set to <NORMAL mode>, the I/O pin is fixed at V_{DD}, and a 8-MHz square wave of amplitude V_{DD}, V_{SS} is input to the OSC1 pin.
- The supply current during operation, I_{DD2}, is measured under the following conditions :
  After reset is released and the oscillation is set to <NORMAL mode>, the I/O pin is fixed at V_{DD}, and a 4-MHz square wave of amplitude V_{DD}, V_{SS} is input to the OSC1 pin.
- The supply current during HALT mode, I_{DD3}, is measured under the following conditions :
  After reset is released and the oscillation is set to <HALT mode>, the I/O pin is fixed at V_{DD}, and a 4-MHz square wave of amplitude V_{DD}, V_{SS} is input to the OSC1 pin.
- During STOP mode, The supply current I_{DD4}, I_{DD5} and I_{DD6} are applied to the circuit other than the auto reset circuit.
- The supply current during STOP mode, I_{DD4}, I_{DD5} are measured under the following conditions :
  After reset is released and the oscillation is set to <STOP mode>, the I/O pin is fixed at V_{DD}, the ACZ pin is fixed at 1/2 V_{DD} and the OSC1 is unconnected.
- The supply current during STOP mode, I_{DD6}, I_{DD7} are measured under the following conditions :
  After reset is released and the oscillation is set to <STOP mode>, the I/O pin is fixed at V_{DD} and the OSC1 is unconnected.

Ta=-40 °C to +85 °C V_{DD}=2.0 V to 5.5 V($V_{RSTL1,2}$ to 5.5 V) V_{SS}=0 V

Parameter		Symbol	Condition	Rating			Unit
				MIN	TYP	MAX	
Input pin NRST (Schmitt input. Pull-up resistor built-in.)							
9	Input high voltage	V_{IH1}		0.8V_{DD}	-	V_{DD}	V
10	Input low voltage	V_{IL1}		V_{SS}	-	0.15 V_{DD}	
11	Input current	I_{I1}	Pull-up resistor ON V_I=1.5 V, V_{DD}=5.0 V	-50	-140	-200	µA
I/O pin P00 to P03(N-ch open-drain output)							
12	Input high voltage	V_{IH2}		0.8V_{DD}	-	V_{DD}	V
13	Input low voltage	V_{IL2}		V_{SS}	-	0.2V_{DD}	
14	Input leakage current	I_{LI2}	V_I=0 V to V_{DD}	-	±0.01	±1	µA
15	Output low voltage	V_{OL2}	I_{OL}=15 mA,V_{DD}=5.0 V	V_{SS}	0.4	1.0	V
I/O pin P10/PWMO0 to P13/PWMO3							
16	Input high voltage	V_{IH3}		0.8V_{DD}	-	V_{DD}	V
17	Input low voltage	V_{IL3}		V_{SS}	-	0.2V_{DD}	
18	Input leakage current	I_{LI3}	V_I=0 V to V_{DD}	-	±0.01	±1	µA
19	Output high voltage	V_{OH3}	I_{OH}=-0.5 mA,V_{DD}=5.0 V	4.5	4.9	V_{DD}	V
20	Output low voltage	V_{OL3}	I_{OL}=15 mA,V_{DD}=5.0 V	V_{SS}	0.4	1.0	
I/O pin P20/AD0, P21/AD1, P22/AD2, P23/AD3 (as port)							
21	Input high voltage	V_{IH4}		0.8V_{DD}	-	V_{DD}	V
22	Input low voltage	V_{IL4}		V_{SS}	-	0.2V_{DD}	
23	Input current	I_{I4}	Pull-up resistor ON V_I=1.5 V, V_{DD}=5.0 V	-50	-140	-200	µA
24	Input leakage current	I_{LI4}	Pull-up resistor OFF V_I=0 V to V_{DD}	-	±0.01	±1	
25	Output high voltage	V_{OH4}	I_{OH}=-0.5 mA,V_{DD}=5.0 V	4.5	4.9	V_{DD}	V
26	Output low voltage	V_{OL4}	I_{OL}=3.5 mA,V_{DD}=5.0 V	V_{SS}	0.1	0.5	

Ta=-40 °C to +85 °C V_{DD}=2.0 V to 5.5 V($V_{RSTL1,2}$ to 5.5 V) V_{SS}=0 V

	Parameter	Symbol	Condition	Rating			Unit
				MIN	TYP	MAX	
I/O pin P30/NSYNC/key0, P31/NIRQ/ACZ/key1, P32/TCO/BZ/key2 (as P30/NSYNC/key0,P31/NIRQ/key1,P32/TCO/BZ/key2, schmitt input)							
27	Input high voltage	V_{IH5}		0.8V_{DD}	-	V_{DD}	V
28	Input low voltage	V_{IL5}		V_{SS}	-	0.1V_{DD}	
29	Input current	I_{I5}	Pull-up resistor ON V_I=1.5 V, V_{DD}=5.0 V	-50	-140	-200	µA
30	Input leakage current	I_{LI5}	Pull-up resistor OFF V_I=0 V to V_{DD}	-	±0.01	±1	
31	Output high voltage	V_{OH5}	I_{OH}=-0.5 mA,V_{DD}=5.0 V	4.5	4.9	V_{DD}	V
32	Output low voltage	V_{OL5}	I_{OL}=3.5 mA,V_{DD}=5.0 V	V_{SS}	0.1	0.5	
Note : When P30/NSYNC/key0 pins are used, output voltage should be over 0.8 VDD at timing signal (NSYNC) output.							
Input pin P31/NIRQ/ACZ/key1 (as ACZ input)							
33	Input high voltage	V_{DHH}	V_{DD} = 4.5 V to 5.5 V figure 1-6-4.	V_{DD}-0.5	-	V_{DD}	V
34	Input low voltage	V_{DLH}		V_{SS}	-	V_{DD}-1.5	
35	Input high voltage	V_{DHL}		1.5	-	V_{DD}	
36	Input low voltage	V_{DLL}		V_{SS}	-	0.5	
37	Input leakage current	I_{LI6}	V_I = 0 V to V_{DD}	-	±0.01	±1	µA
38	Input clamp current	I_{CL6}	V_I > V_{DD}, V_I < 0 V	-	-	±500	
39	Rise time	trs	figure 1-6-4.	30	-	-	µs
40	Fall time	tfs		30	-	-	

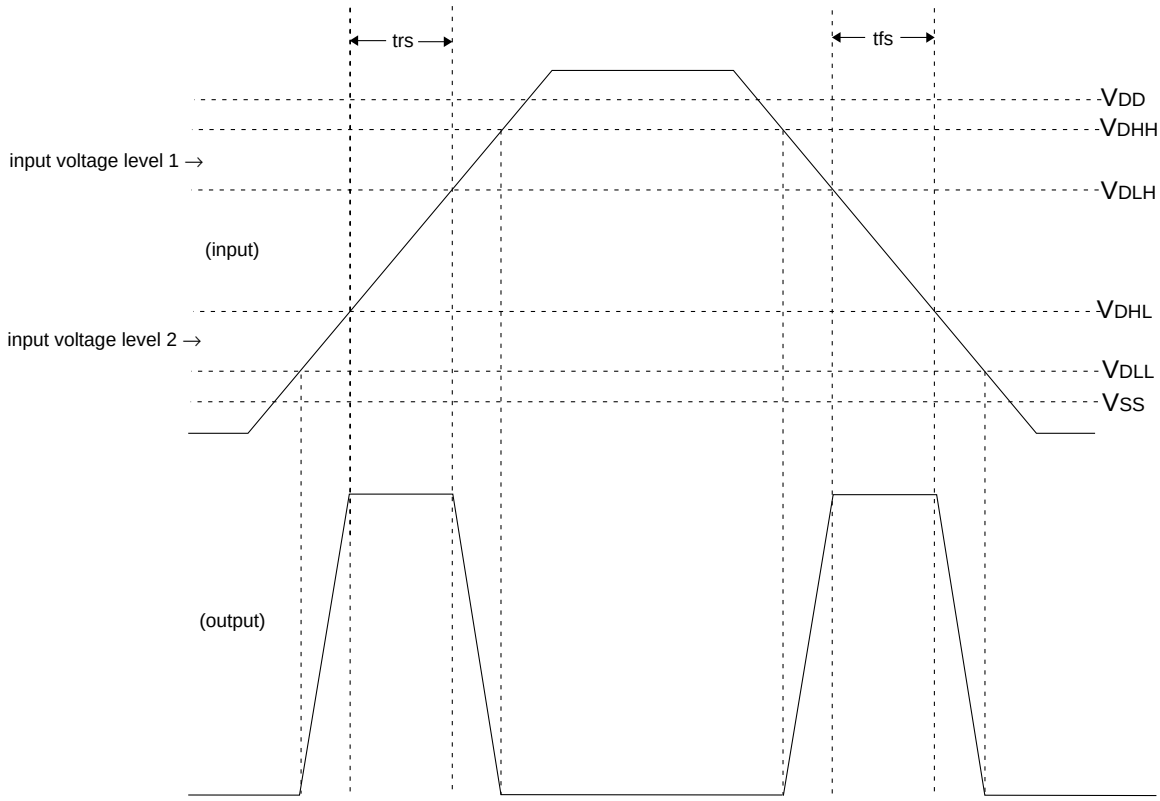


Figure 1-6-4 AC Zero-cross Detection Circuit Operation

1-6-4 A/D Converter Characteristics

Ta = -40 °C to +85 °C V_{DD} = 2.0 V to 5.5 V($V_{RSTL1,2}$ to 5.5 V) V_{SS} = 0 V

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
1	Resolution			-	-	10	Bits
2	Non-linearity error		V_{DD}=5.0 V, V_{SS}=0.0 V fosc=8 MHz (divided by 8) T_{AD}=1.0 µs, T_S=2.0 µs	-	-	±3	LSB
3	Differential non-linearity error			-	-	±3	LSB
4	Zero transition voltage	V_{DT}	V_{DD}=5.0 V V_{SS}=0.0 V	-	10	30	mV
5	Full-scale transition voltage	V_{FST}		4950	4980	-	mV
6	A/D conversion time		fosc=8 MHz (divided by 8) T_{AD}=1.0 µs	12.0	-	28.0	µs
7	Sampling time	T_S		2.0	-	18.0	µs
8	Analog input voltage	V_{IA}		V_{SS}	-	V_{DD}	V
9	Analog input leakage current	I_{LIA}	When channel OFF V_I=0 V to V_{DD}	-	±0.01	±1	µs
10	Ladder resistance	R_{ladd}		10	30	100	kΩ

- Zero transition voltage

  It indicates how much difference between the nominal value and the analog input voltage, when digital output code is changed from "0" to "1" (x'000' → x'001').

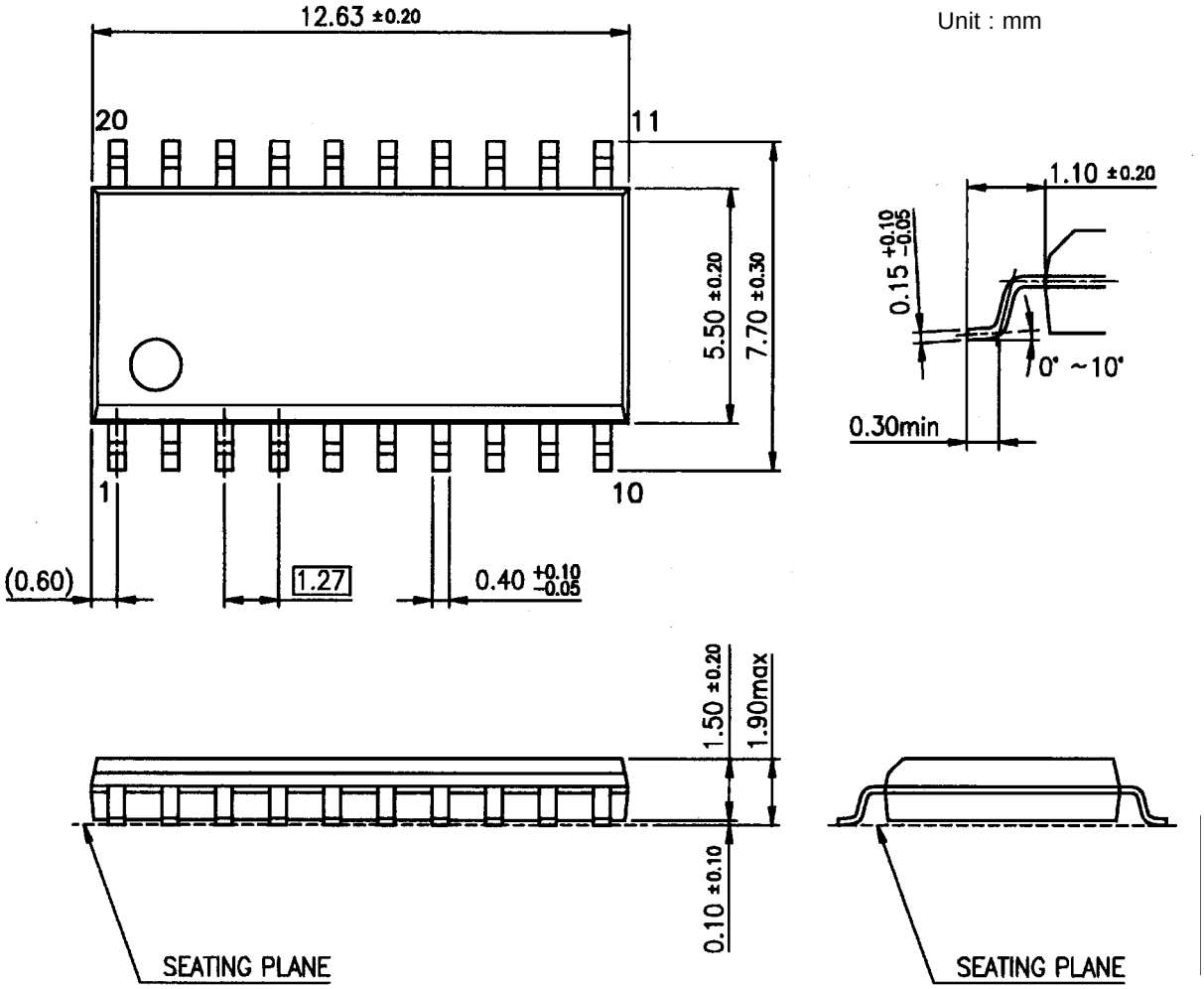
- Full-scale transition voltage

  It indicates how much difference between the nominal value and the analog input voltage, when digital output code reached the full-scale (x'3FE' → x'3FF') .

1-7 External Dimensions

Package code :＊SOP020-P-0300D

Unit : mm



＊SOP020-P-0300D is Pb free package.
Conventional package is ＊SOP020-P-0300

The package dimension is subjected to change. Before using this product, please obtain product specifications from the sales office.

1-8 Option

1-8-1 Mask Option

This LSI has the following mask option.

- Automatic reset circuit setup
  Select automatic reset circuit from among the automatic reset circuit 1, the automatic reset circuit 2, and "unused".

1-8-2 Mask Option Form (VER 0.05)

SE No. Date :

Model name	MN15G 02	Customer		Approval	

1. Power supply current and voltage

	voltage	used	not used
at operation	V to V		
HALT mode	V to V		
STOP mode	V to V		

2. Automatic reset circuit

		When it is used, check the applicable item. →				
Used			Reset voltage	V_{RSTL1}	3.2 V to 4.4 V	
Unused				V_{RSTL2}	1.6 V to 2.5 V	

V_{RSTL2} cannot be selected at tc (the instruction execution time) < 2 µs.

Chapter 2 Basic CPU

2-1 Clock Generator

2-1-1 Clock Generator

This LSI has internal oscillator circuit for generating system clock (OSC1, OSC2). This circuit requires external oscillators and capacitors. Connect a crystal or ceramic oscillator (Figure 2-1-1) to it.

> To minimize distortion, mount the oscillator and capacitor as close as possible to the pins. Also connect the Vss pin to a thick ground line with shortest possible distance to prevent noise and to stable oscillation. The best value of capacitor depends on oscillator, refer to the value specified by each manufacturer.

■Oscillator circuit connection

Figure 2-1-1 provides oscillator circuit connections.

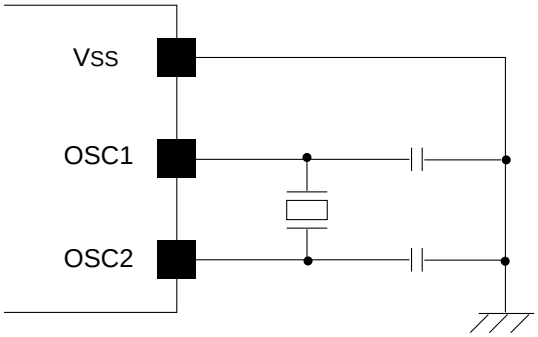


Figure 2-1-1 Oscillator circuit connection

2-1-2 CPU Basic Timing

Source oscillation generates 4 clocks (S0, S1, S2, S3) to form machine cycle (state). At 4.0 MHz, 1 machine cycle is 1.0 µs at divided by 4, and 2.0 µs at divided by 8.

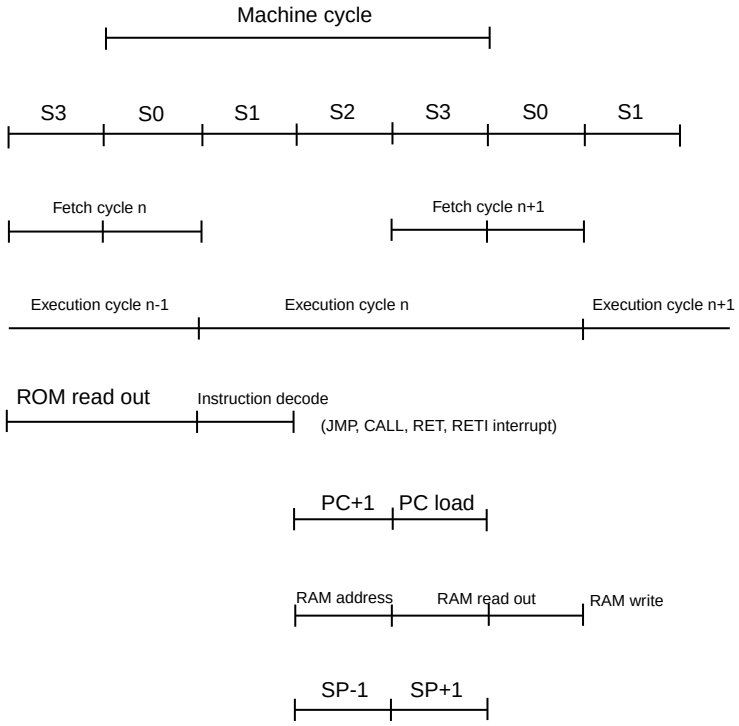


Figure 2-1-2 Machine Cycle and CPU Basic Timing

2-2 Register Set

This LSI has register for operation, for pointer and for store.

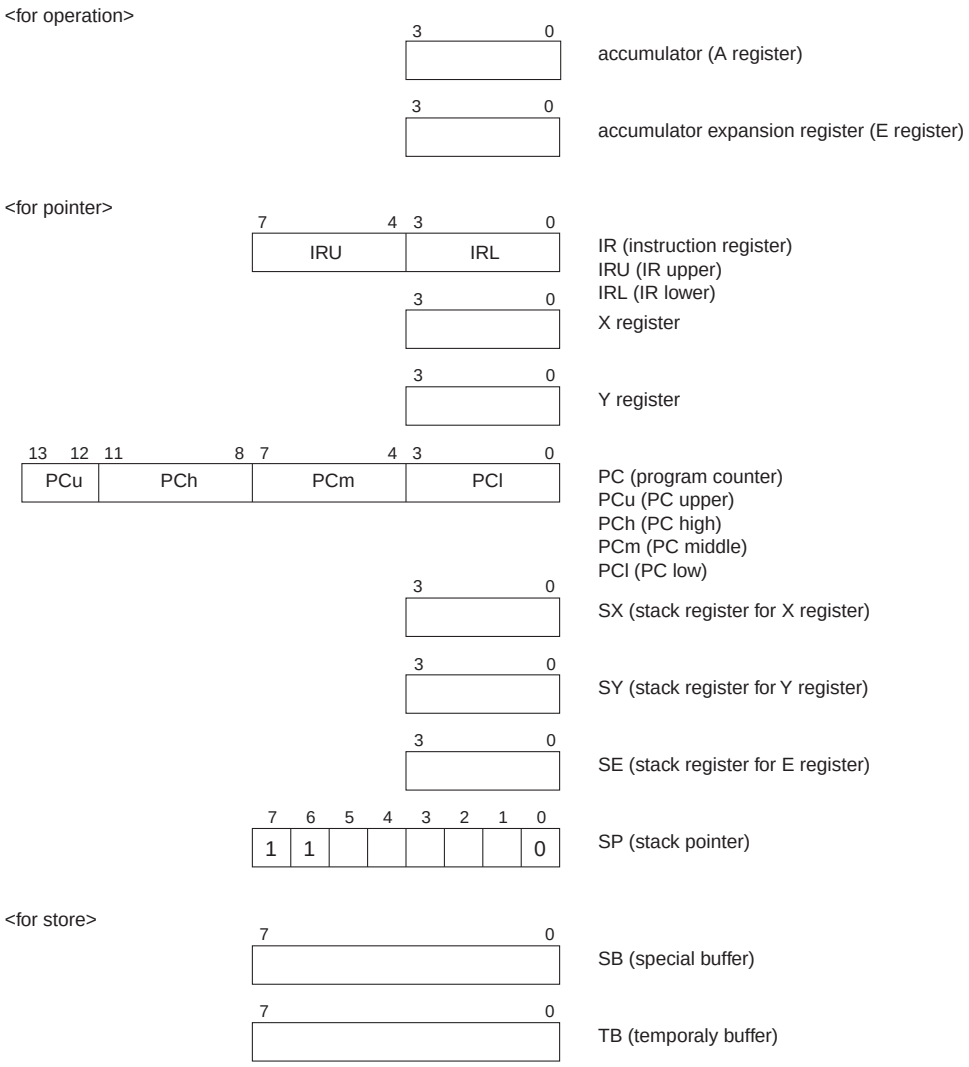
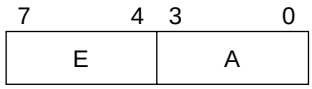


Figure 2-2-1 CPU Control Registers

■Accumulator (A register)
This register can be used generally for all operations.

■Accumulator expansion register (E register)
This register can be used generally for operation. At transfer instruction of 8-bit data, this register can be used for upper 4 bits or RAM odd address.



---

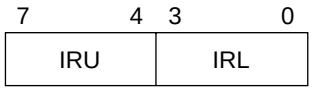
ex.

STBD (store byte direct)

M (da + 1) ← E M (da) ← A

Data in E register and accumulator are transferred to the address in RAM, specified directly (da). Data in E register is transferred to odd address (da + 1), data in accumulator is transferred to even address (da).

■Instruction register (IR)
This register reads out the instruction that CPU is going to execute, from ROM and latches.



■Program counter (PC)
This register controls the execution order of instructions in program memory.
PCu should be set to "0".

■X register

This register is 4-bit register, indirectly specifies RAM area. It specifies upper 4 bits of RAM address (X, Y).

■Y register

This register is 4-bit register, indirectly specifies RAM area. It specifies lower 4 bits of RAM address (X, Y).

■Stack register for X register (SX)

This is RAM for X register to stack. It can be used as normal RAM.

RAM address X (0, 0)

■Stack register for Y register (SY)

This is RAM for Y register to stack. It can be used as normal RAM.

RAM address X (0, 0)

■Stack register for E register (SE)

This is RAM for E register to stack. It can be used as normal RAM.

RAM address X (0, 2)

■Flag status

Two flags (CF and ZF) reflect operation's results. LIFF reflects LI instruction execution status.

CF (Carry Flag)
The carry flag is set when ALU operation results is an overflow or an underflow. Otherwise, it is reset.

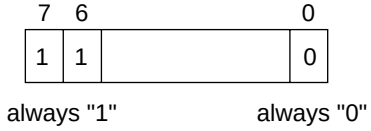
ZF (Zero Flag)
The zero flag is set when ALU operation results is zero. Otherwise, it is reset.

LIFF (Load Immediate Flag)
This memorizes that the last instruction is LI instruction. It is used to

Instruction	LIFF	Description
NOP	0	no execution
LI 5	0	Set 5 to accumulator
LI 8	1	no execution
LI 9	1	no execution
OUT 0, X'F'	0	Output 5 to port 0

■Stack Pointer (SP)

This is a 8-bit register that indicates address of stack area in data RAM. Stack area is used for PC to stack at subroutine call and at interrupt.



■Special Buffer (SB)

This register can input / output data by 8-bits, by RDSB, WTSB instruction, between E register and A register.

■Temporary Buffer (SB)

This register can input / output data by 8-bits, by RDBC, WTTB instruction, between E register and A register.

2-3 Memory Space

This LSI has independently, an instruction memory area (ROM) that stores instructions and a data memory area (RAM : include stack area) that stores data. ROM can be used as a memory for stable data such as table data.

2-3-1 ROM Address Space (2 KB)

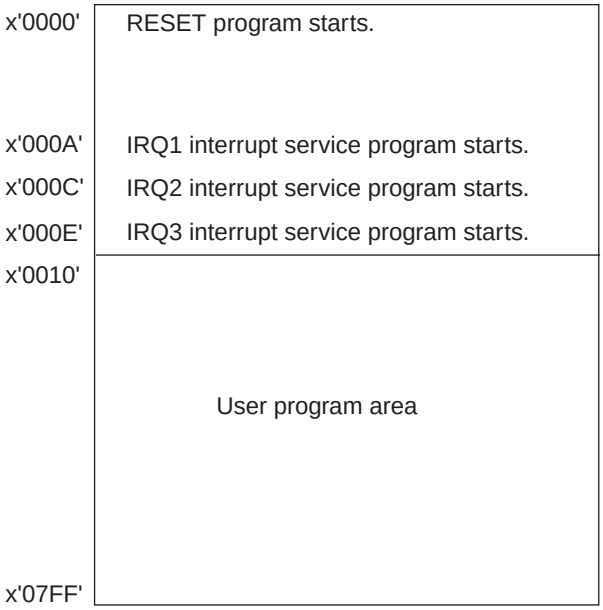
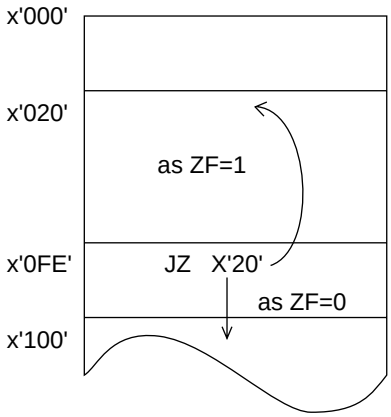


Figure 2-3-1 ROM Address Space

ROM address can be specified by program counter, E register or accumulator. 1 page for 256 byte and ROM is divided by maximum 8 pages.

■Direct address in page (ex. JZ, JNZ instruction)
Address that is directly specified in instruction code indicates the branched address in the same page.



■Direct address 1 (ex. JMP, CALL instruction)
Address that is directly specified in instruction code indicates the branched address for no condition. or of subroutine. Directly specified address is 12-bit (PCh, PCm, PCl), an arbitrary address can be specified.

■Direct address 2 (ex. JMPL, CALLL instruction)
Address that is directly specified in instruction code indicates the branched address for no condition. or for subroutine. PCu should be set to "0".

■Special address in zero page (x'0000' to x'00FF') (ex. CALS instruction)
Address that is specified in instruction code indicates the branched address for subroutine by 16 byte in zero page.

■Accumulator indirectly address (ex. JMPEA instruction)
Address that is specified in 4 bit of E register (upper address) and in 4 bit of A register (lower address) indirectly indicates the branched address for no condition. That is branched in the same page.

■Cautions on the branch instruction with condition (JC, JNC, JZ, JNZ, JBZ, JBNZ, CYIJ)
Conditional branch instruction is branched to the address that is indicated in 2 byte of instruction in the same page, if condition is set. At the border of page, jump address is to the next page.

ex. JC

Address	Machine code	
000 . . . 015 . . . 0FE 0FF	 6F 15	 jc xxx
100 . . . 115 . . . 1FF		←2 ←3

←1

← PCh(PC8 to PC11) is changed here.

As shown the above example, if JC instruction is located from x'0FE' to x'0FF' it is branched to the address that is indicated in 2 when condition is set. And when condition is not set, it is executed the instruction of the address (x'115') that is indicated in 3.

2-3-2 ROM Address Space (4KB)

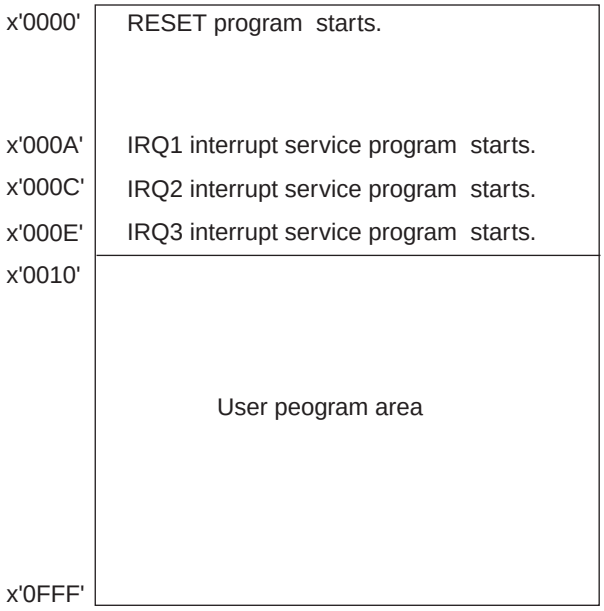
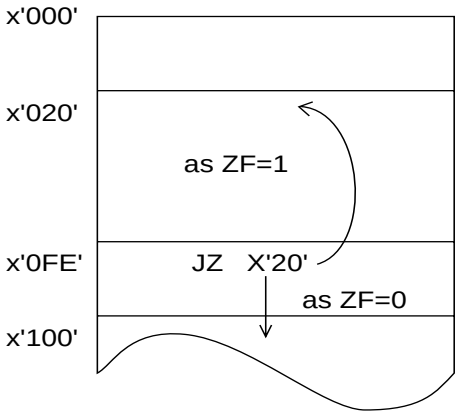


Figure 2-3-2 ROM Address Space

ROM address can be specified by program counter, E register or accumulator. 1 page for 256 byte. It is divided by maximum 16 pages.

■Direct address in page (ex. JZ, JNZ instruction)
Address that is directly specified in instruction code indicates the branched address in the same page.



■Direct address 1 (ex. JMP, CALL instruction)
Address that is directly specified in instruction code indicates the branched address for no condition. or of subroutine. Directly specified address is 12-bit (PCh, PCm, PCl), an arbitrary address can be specified.

■Direct address 2 (ex. JMPL, CALLL instruction)
Address that is directly specified in instruction code indicates the branched address for no condition. or for subroutine. PCu should be set to "0".

■Special address in zero page (x'0000' to x'00FF') (ex. CALS instruction)
Address that is specified in instruction code indicates the branched address for subroutine by 16 byte in zero page.

■Accumulator indirectly address (ex. JMPEA instruction)
Address that is specified in 4 bit of E register (upper address) and in 4 bit of A register (lower address) indirectly indicates the branched address for no condition. That is branched in the same page.

■Cautions on the branch instruction with condition (JC, JNC, JZ, JNZ, JBZ, JBNZ, CYIJ)
Conditional branch instruction is branched to the address that is indicated in 2 byte of instruction in the same page, if condition is set. At the border of page, jump address is to the next page.

ex. JC

Address	Machine code	
000 . . . 015 . . . 0FE 0FF	 6F 15	 ←1 jc xxx
100 . . . 115 . . . 1FF		←2 ←3

← PCh(PC8 to PC11) is changed here.

As shown the above example, if JC instruction is located from x'0FE' to x'0FF', it is branched to the address that is indicated in 2 when condition is set. And when condition is not set, it is executed the instruction of the address (x'115') that is indicated in 3.

2-3-3 RAM Address Space

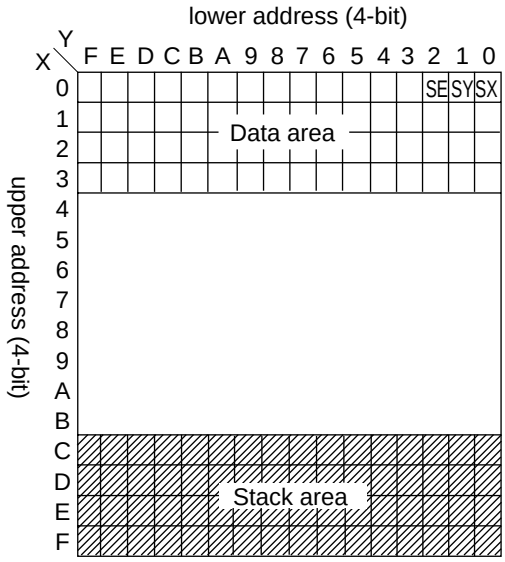


Figure 2-3-3 RAM Address Space

2-3-4 Stack Area

Stack area is allocated from x'C0' to x'FF' in RAM area. Stacked area is used for program counter, flag status (ZF,CF), accumulator, E, X, Y registers to stack at CALL instruction, PSH instruction and at interrupt. When the whole area is not used as stacked area, it can be used as a normal RAM. If only CALL instruction is used, the maximum 16 levels can be used.

Figure 2-3-4 shows the status of stack area when CALL, PSH instructions and interrupt sequence are executed.

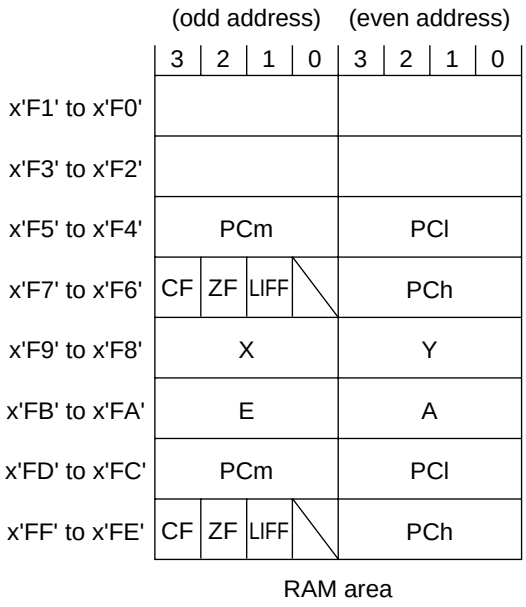


Figure 2-3-4 Status of Stacked Area

■SP (Stack Pointer) shows x'C0' at reset. Also stacked data is used from x'FF' to x'C0' in order.

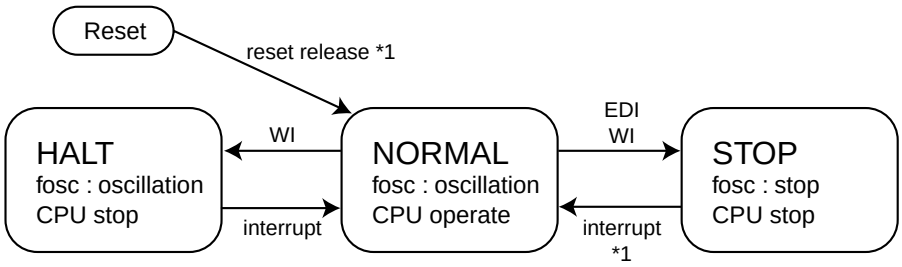
■In RET instruction, flags (CF, ZF, LIFF) are not recovered. Only RETI instruction is recovered.

■LIFF memorizes that the last instruction is LI instruction. It is used to pile up instructions.

2-4 Clock Switching

2-4-1 Clock Switching

This LSI can be switched the system clock division factor by instruction. The CLKSEL1 flag of the CPU mode register (CPUM) switches the division factor of the system clock (Figure 2-4-1). At fosc=4.0 MHz, instruction cycle is 1.0 µs at divided by 4, and 2.0 µs at divided by 8. NORMAL mode means the mode that CPU is operated. As shown on figure 2-4-1, at reset, the CLKSEL1 is "0", NORMAL mode is selected and operation is started from the reset cycle.



*1 fosc oscillation stabilization waiting time is needed on hardware.

Figure 2-4-1 CPU Operation Mode and Setup

2-4-2 CPU Mode Register

This is readable / writable register that switches the division rate of the system clock.

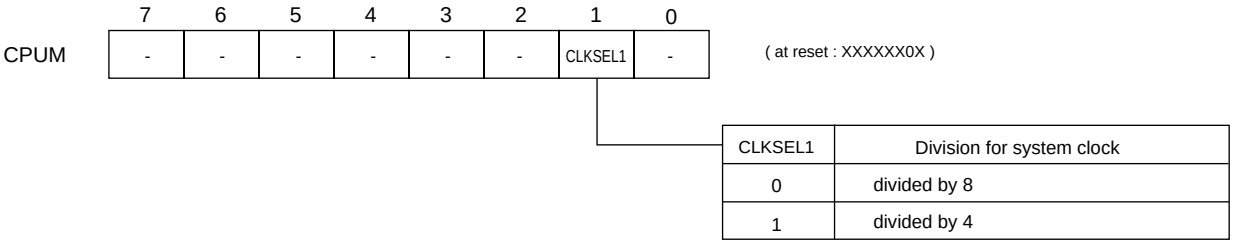


Figure 2-4-2 CPU Mode Register (CPUM : x'030', R/W)

Table 2-4-1 Status of Operation Mode

Mode	Operation clock	System clock (fsys)	CPU
	OSC1 / OSC2 (fosc)		
NORMAL	Oscillation	fosc/8 or fosc/4	Operate
HALT	Oscillation	fosc/8 or fosc/4	Stop
STOP	Stop	Stop	Stop

2-5 Back Up Mode

There are two back up mode to save electric consumption. They can be controlled by program.

HALT mode : The system clock is supplied. It is recovered by a reset or by an interrupt.
STOP mode : The division circuit for the system clock is stopped, so that the electric consumption is more saved. It is recovered by a reset or by an interrupt.

Table 2-5-1 STOP / HALT Functions

Mode / Description	STOP	HALT
Operation status	1) System clock oscillation circuit stop.	1) System clock oscillation circuit operates (dividing circuit for system clock operates) 2) Timer count operates
Mode setup	WI instruction is executed soon, after EDI instruction is done. (refer to ex.)	WI instruction is executed soon, after instruction (except EDI) is done. (refer to ex.)
Recover	- interrupt same as a normal interrupt - reset same as a normal reset	

---

ex.

STOP mode usage example

When IRQ1 (interrupt 1) is generated, it is recovered from STOP mode.

To stable the operation, more than 1 NOP should be inserted after EDI, WI instructions.

```
EDI     0, 4    ;
WI              ;
NOP             ;
```

There are 2 interrupts that can be recovered from STOP mode.

- Interrupt 1 (IRQ1)
- Interrupt 3 (IRQ3) (except timer 3)

---

ex.

HALT mode usage example

```
        EDI                 0, 7        ; Even any interrupt is generated, that can be recovered from HALT mode.
        (instructions except EDI) ;
        WI                              ;
        NOP                             ;
```

There are 3 interrupts that can be recovered from HALT mode.

- Interrupt 1 (IRQ1)
- Interrupt 2 (IRQ2)
- Interrupt 3 (IRQ3)

More than 1 NOP should be inserted after WI instruction. In cross assembler we offer, NOP is automatically inserted.

2-5-1 Cautions on Back Up Mode

■I/O port

Pull-up resistance for pins at high-impedance should be set by the software with corresponding the voltage level of external circuit at backup, to save the electric consumption at port . Set the voltage level of the input port to "H" level or "L" level. If the level is middle, micro controller spend much more the electric consumption.

■Recover from STOP mode

If the power supply voltage is less than 1.8 V at recover, RAM data after recover may be damaged. In this case, reset by the external circuit.

2-6 Reset

2-6-1 Reset Operation

The CPU contents are reset when the NRST pin is pulled to low from external, or outputs "L" level by overflow of watchdog timer, by low voltage detector of auto-reset circuit. When a reset is generated, registers and data memory is initialized.

Auto-reset circuit is mask option.

Table 2-6-1 Initial Value of Register / Memory

Register / Memory		Symbol	Initial value
1	Program counter	PC	0
2	accumulator	A	0
3	E register	E	0
4	X register	X	0
5	Y register	Y	0
6	Carrier flag	CF	0
7	Zero flag	ZF	0
8	Special buffer	SB	indefinite
9	Temporary buffer	TB	indefinite
10	RAM		indefinite
11	Stack pointer	SP	0
12	Interrupt flag	IF	0
13	Interrupt enable / disable flag	IE	disable
14	Port data register		1
15	Port control register		0
16	Control register	CR	0

Some registers can not be set to "0".
For detail, refer to instructions of each register.

■Initiating a reset

The CPU contents are reset when the NRST pin is pulled to low from external, or outputs "L" level by overflow of watchdog timer, low voltage detector of auto-reset circuit. For stable reset, the NRST pin should keep "L" for more than 1 machine cycle.

■Timing of reset release

After the NRST pin becomes "H", there is 2^{14} pulse counts of OSC input clock (fosc). The period from counting to overflow is called "oscillation stabilization wait time". This period is automatically inserted at reset release, at recover from STOP mode. This is happened because, if the internal reset is released when source oscillation of the system clock is unstable, micro controller may be wrongly operated. After oscillation stabilization wait time is finished, internal reset is released and program is started from the address x'0000'.

This LSI starts form NORMAL mode.

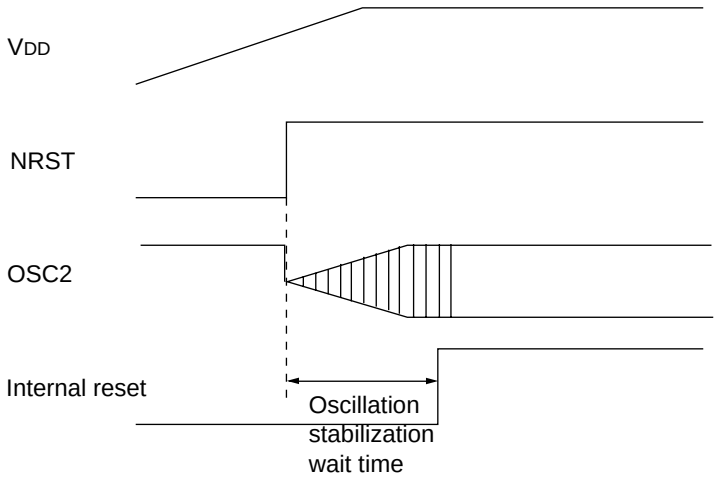


Figure 2-6-1 Reset Released Sequence

At internal reset, P30 / NSYNC / key 0 pin outputs the system clock (S0).

When the auto-reset circuit is selected in mask option, the circuit that has enough time of "L" level pulse should be used.

Chapter 3 Portts

3

3-1 Overview

3-1-1 Port Diagram

There are four ports, port 0, port 1, port 2 and port 3. Each port is assigned to its corresponding special function register area in memory.

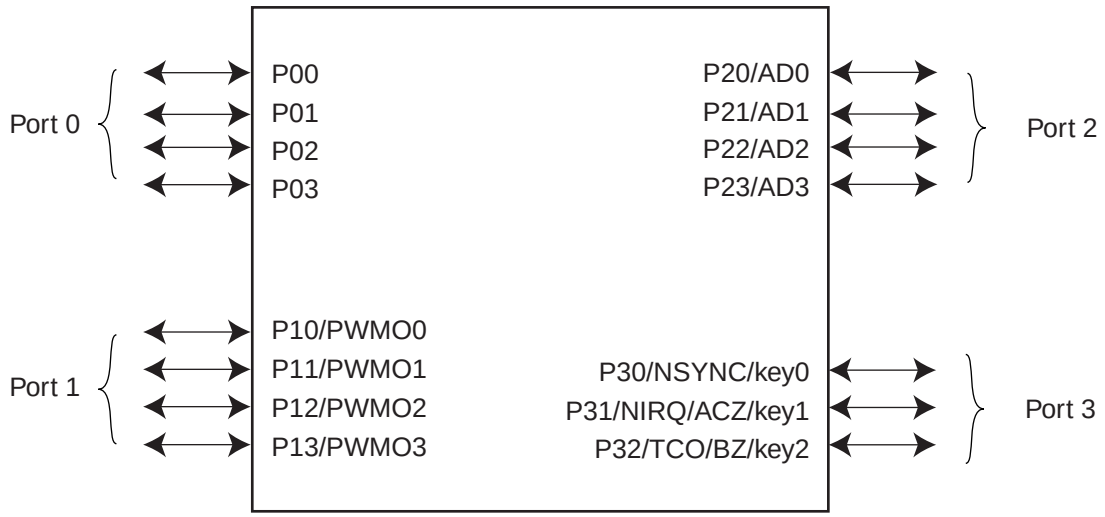


Figure 3-1-1 Port Functions

3-1-2 Port Functions

Table 3-1-1 Port Functions

Port		Dual function	I/O	I/O control		Pull-up resistor		Output structure control	
				Function	at reset	Function	at reset	Function	at reset
Port 0	P00 P01 P02 P03	- - - -	I/O	Each bit can be set individually as either an input or output.	Input	-	-	-	-
Port 1	P10 P11 P12 P13	PWMO0 PWMO1 PWMO2 PWMO3	I/O	Each bit can be set individually as either an input or output.	Input	-	-	Output structure can be selected individually on each bit.	CMOS output
Port 2	P20 P21 P22 P23	AD0 AD1 AD2 AD3	I/O	Each bit can be set individually as either an input or output.	Input	Pull-up resistor can be set individually on each bit.	No resistor	Output structure can be selected individually on each bit.	CMOS output
Port 3	P30 P31 P32	NSYNC key0 NIRQ ACZ key1 TCO BZ key2	I/O	Each bit can be set individually as either an input or output.	Input	Pull-up resistor can be set individually on each bit.	No resistor	Output structure can be selected individually on each bit.	CMOS output

3-1-3 Port Status at Reset

Table 3-1-2 Port Status at Reset

Port	I/O mode	Pull-up resistor
Port 0	Input mode	-
Port 1	Input mode	-
Port 2	Input mode	No pull-up resistor
Port 3	Input mode	No pull-up resistor

P30/NSYNC/key0 outputs the system clock (s0) at internal reset.

3-1-4 Port Disposal at Unused

Disposal of unused pins should be considered the status at reset. Table 3-1-3 shows the disposal.

Table 3-1-3 Disposal of Unused Pins

Pin's type	Port	Unused pin
I/O pin	Port 0	OPEN
	Port 1	OPEN
	Port 2	OPEN
	Port 3	Pull-up or pull-down should be added. *1

*1 When the internal resistor is used, the through current is happened till the setup complete.

3-1-5 Setup Example

■Setup example

A setup example of input / output port by port 2, port 3. Port 3 is input port. Port 2 in output port. Pull-up resistor is added to port 3, not to port 2.

An example setup procedure, with description of each step is shown below.

Setup Procedure	Description
(1) Control the I/O direction of port. P23DIR (x'012') bp6-4 :P3DIR2-0 = 000 bp3-0 :P2DIR3-0 = 1111	(1) Set the P3DIR2-0 flag of theP23DIR register to "000" to set port 3 to input port. Set the P2DIR3-0 flag to "1111" to set port 2 to output port.
(2) Add pull-up resistor. P23PLU (x'022') bp6-4 :P3PLU2-0 = 111 bp3-0 :P2PLU3-0 = 0000	(2) Set the P3PLU2-0 flag of theP23PLU register to "111" to add pull-up resistor to port 3. Set the P2PLU3-0 flag to "0000" not to add pull-up resistor to port 2.

Port 2 outputs data when lower 4 bits of port 2, port 3 data register (PORT23) are written, and OUT instruction is executed. The status of port 3 can be input when upper 4 bits of port 2, port 3 data register (PORT23) are read, and IN instruction is executed.

3-1-6 Control Registers

I/O port control register includes a data register (PORTn) that outputs data, a direction control register (PnDIR) that controls I/O direction, a pull-up resistor control register (PnPLU) that controls pull-up resistor and output structure control register (PnSC) that controls output structure.

Table 3-1-4 Port Control Registers List

	Register	Address	R/W	Function	Page
Port 0 Port 1	PORT01	x'000'	R/W	Port 0, port 1 data register	Ⅲ - 9
	P01DIR	x'010'	R/W	Port 0, port 1 direction control register	Ⅲ - 9
	P01SC	x'028'	R/W	Port 1 output structure control register	Ⅲ - 9
Port 2 Port 3	PORT23	x'002'	R/W	Port 2, port 3 data register	Ⅲ - 13
	P23DIR	x'012'	R/W	Port 2, port 3 direction control register	Ⅲ - 13
	P23PLU	x'022'	R/W	Port 2, port 3 pull-up resistor control register	Ⅲ - 13
	P23SC	x'02A'	R/W	Port 2, port 3 output structure control register	Ⅲ - 14

R/W : Readable / Writable

Access to x'010' to x'02A' can be available only by 8-bit

3-2 Port 0, 1

3-2-1 Description

■General Port Setup

Each bit can be set individually as either an input or output by the port 0, port 1 I/O direction control register (P01DIR). The control flag of the port 0, port 1 direction control register (P01DIR) is set to "1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the direction control register (P01DIR) to "0", or set the output configuration to "N-ch open drain" by the output structure control register (P01SC) and set the port 0, port 1 data register (PORT01) to "1" to select "Hi-z output", then read the value of the port 0, port 1 data register (PORT01).

To read input data, the pin's status should be read, not the value of the PORT01 register.

To output data to pin, set the control flag of the direction control register (P01DIR) to "1" and write the value of the port 0, port 1 data register (PORT01).

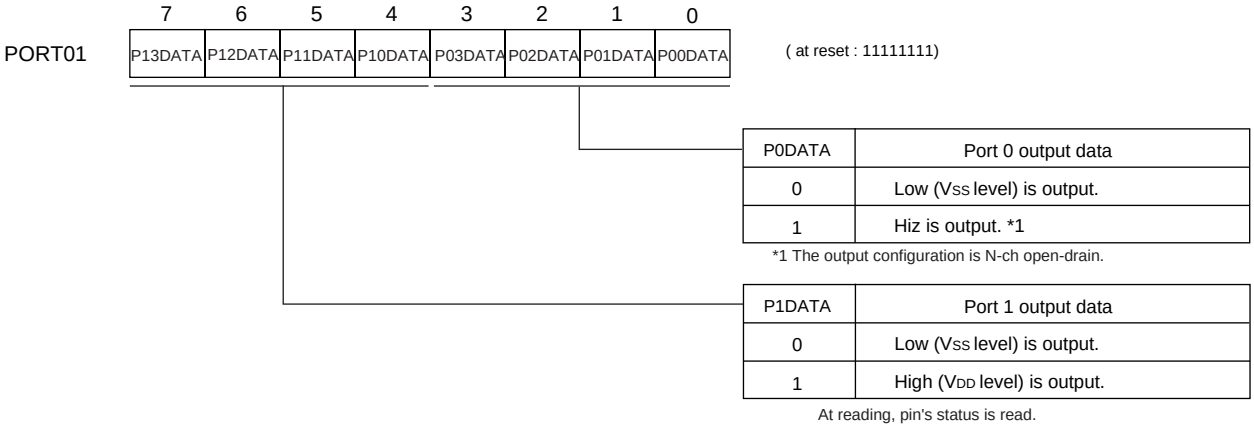
Each bit can be set individually the output configuration by the port 1 output structure control register (P01SC). Set the control flag of the port 1 output structure control register (P01SC) to "1" for N-ch open-drain, and to "0" for CMOS output.

The output structure of port 0 is N-ch open-drain.
When the port 0, 1 register is written to "1", it becomes high impedance output.

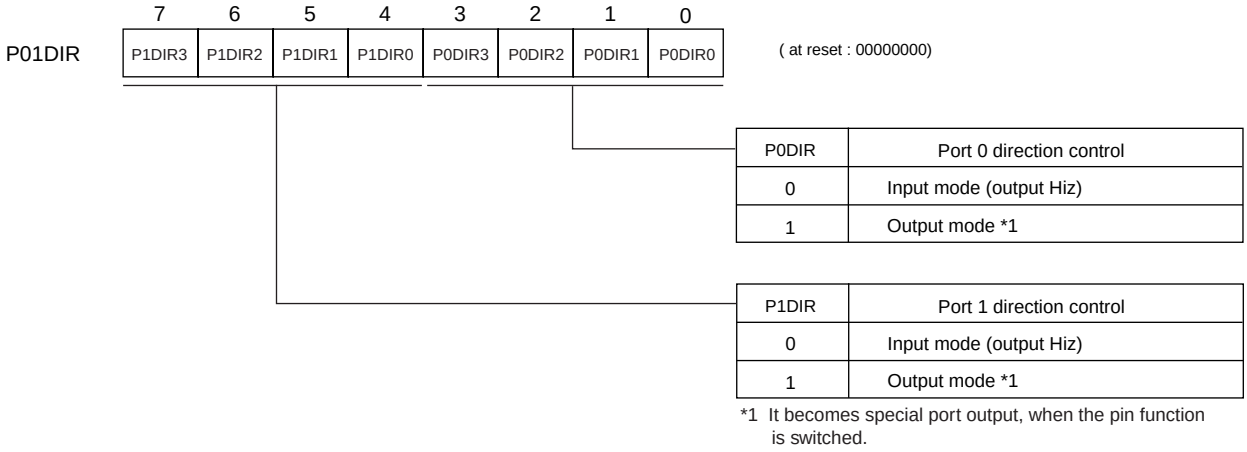
■Special Function Pin Setup

P10 to P13 are used as PWM output pin (General port : at reset). Each bit can be set individually if the PWM output is enabled or not, by the buzzer output control register (BZCTR). When it is enabled, the conjunction of the port 1 output data and the timer output that the timer control input control register (MODCNT) selects, is output to pin.

3-2-2 Registers



Port 0, Port 1 Data Register (PORT01 : x'000', R/W)



Port 0, Port 1 Direction Control Register (P01DIR : x'010', R/W)

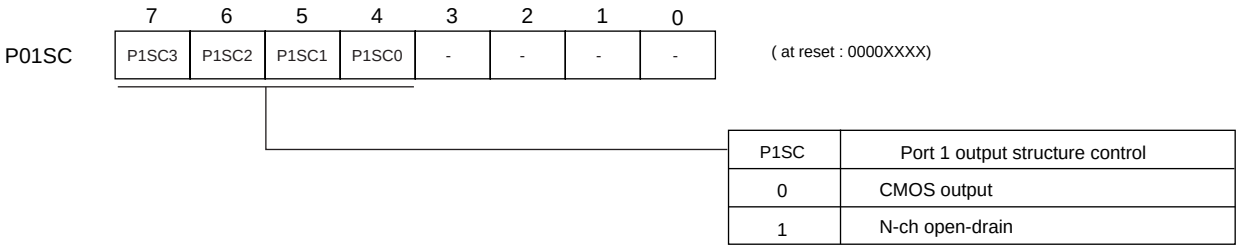


Figure 3-2-1 Port 0, Port 1 Registers

3-2-3 Block Diagram

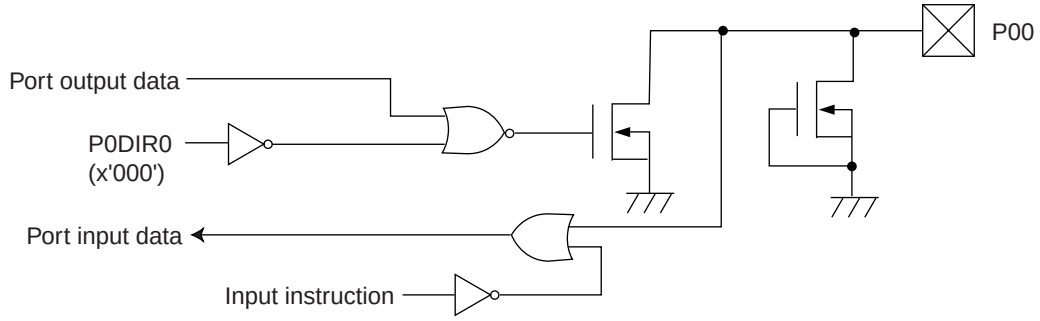


Figure 3-2-2 Block Diagram (P00)

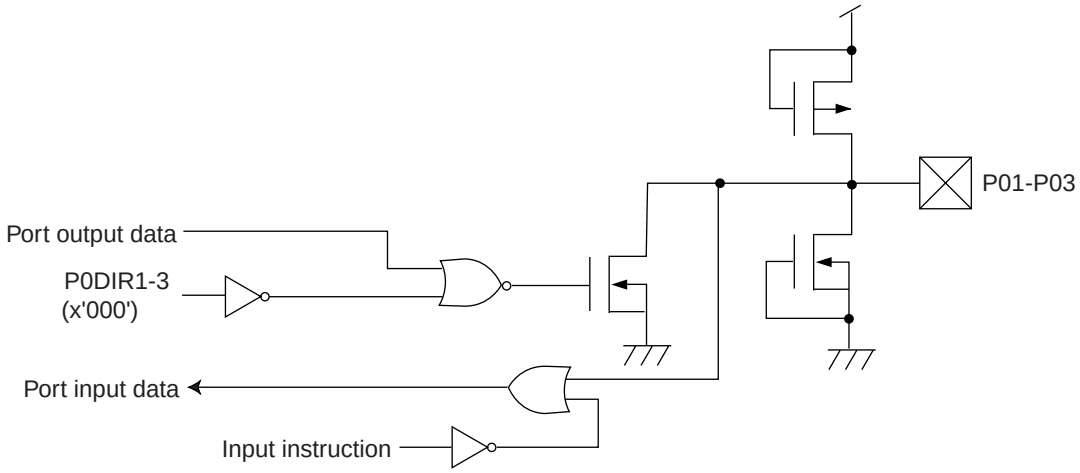


Figure 3-2-3 Block Diagram (P01, P02, P03)

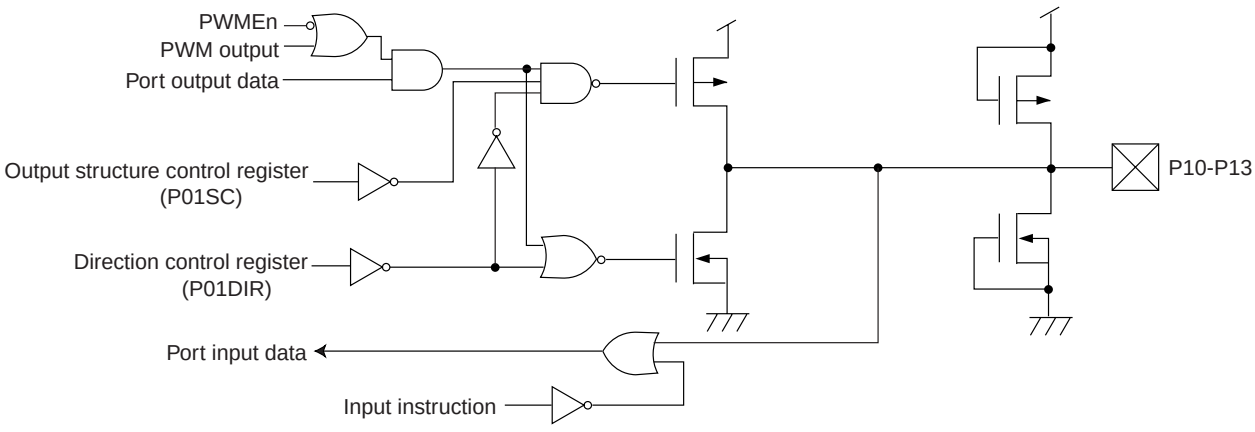


Figure 3-2-4 Block Diagram (P10, P11, P12, P13)

3-3 Port 2, 3

3-3-1 Description

■General Port Setup

Each bit can be set individually as either an input or output by the port 2, port 3 I/O direction control register (P23DIR). The control flag of the port 2, port 3 direction control register (P23DIR) is set to "1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the direction control register (P23DIR) to "0" or set the output configuration to "N-ch open drain" by the output structure control register (P23SC) and set the port 2, port 3 data register (PORT23) to "1" to select "Hi-z output", then read the value of the port 2, port 3 data register (PORT23).

To read input data, the pin's status should be read, not the value of the PORT23 register.

To output data to pin, set the control flag of the direction control register (P23DIR) to "1" and write the value of the port 2, port 3 data register (PORT23).

Each bit can be set individually if pull-up resistor is added or not, by the pull-up resistor control register (P23PLU). Set the control flag of the pull-up resistor control register (P23PLU) to "1" to add pull-up resistor.

Each bit can be set individually the output configuration by the port 1 output structure control register (P23SC). Set the control flag of the port 1 output structure control register (P23SC) to "1" for N-ch open-drain, and to "0" for CMOS output.

■Special Function Pin Setup

P20 to P23 are used as analog input pin (AD0 to AD3) (General port : at reset). Set pin to input mode by the port 2, port 3 direction control register (P23DIR) and set the port 2, port 3 output structure control register (P23PLU) to "0" to select pull-up resistor "OFF".

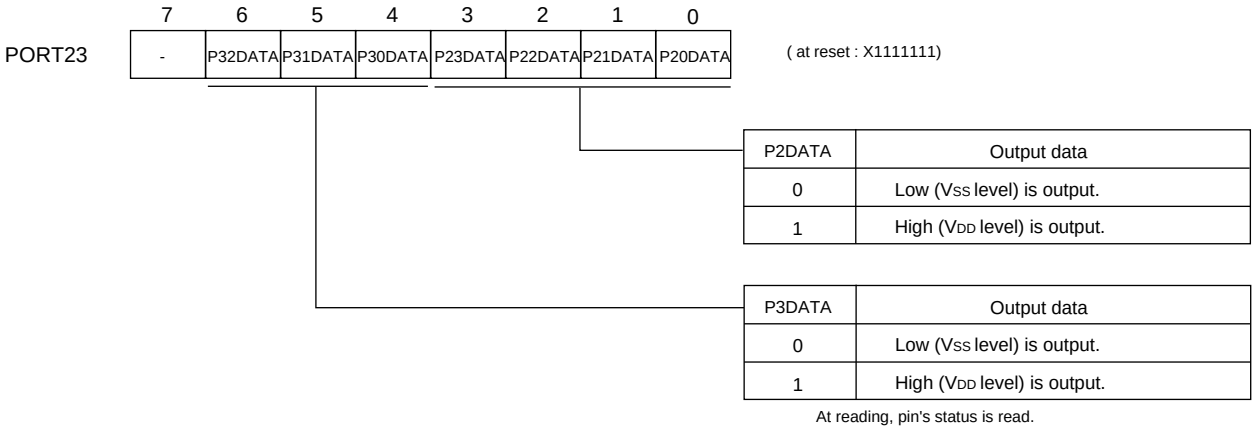
P30 is used as system clock synchronous output (NSYNC) (General port : at reset). NSYNC output outputs the synchronous signal of the system clock at internal reset.

P31 is used as interrupt input (NIRQ), AC zero-cross detection input (ACZ) (General port : at reset). NIRQ is input pin of interrupt 1. Set P31 to input mode. At operation, the initial status is P31, but the ACZCNT register can switch NSYNC output / port data output. AC zero-cross detection input (ACZ) is input pin of AC zero-cross circuit. ACZCNT register can switch port input data / ACZ input.

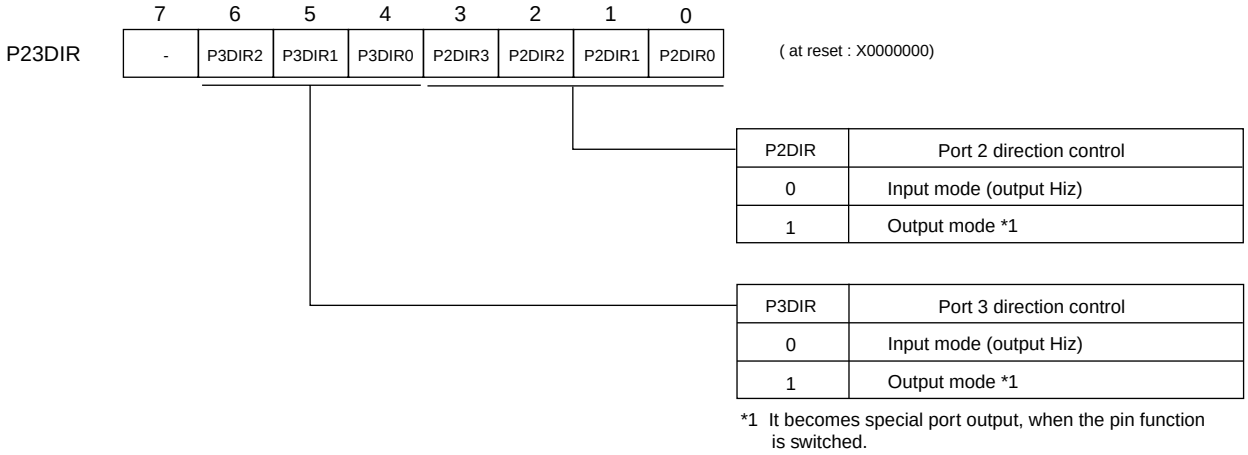
P32 is used as timer output (TCO), and as buzzer output (BZ) (General port : at reset).
TCO is timer output pin. TCOCNT register can switch timer output / port data output.
BZ is buzzer output pin. BZCTR register can switch buzzer output / port data output.

Also, P30, P31 and P32 are used as key interrupt. When key interrupt input is used, enable key interrupt by the key interrupt control register 1 (KEYCNT). Set pin to input mode by the port 2, 3 direction control register (P23DIR), and add pull-up resistor if necessary.

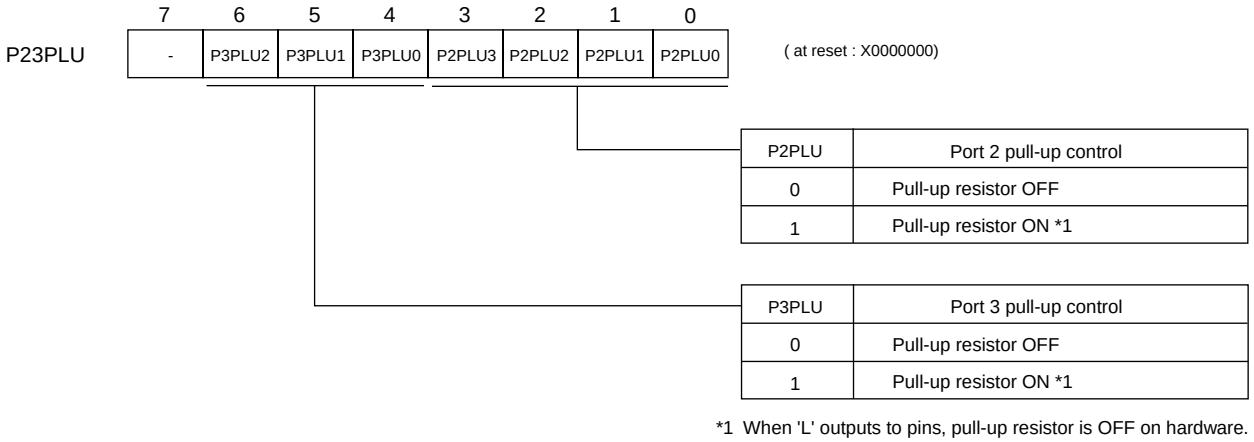
3-3-2 Registers



Port 2, Port 3 Data Register (PORT23 : x'002', R/W)

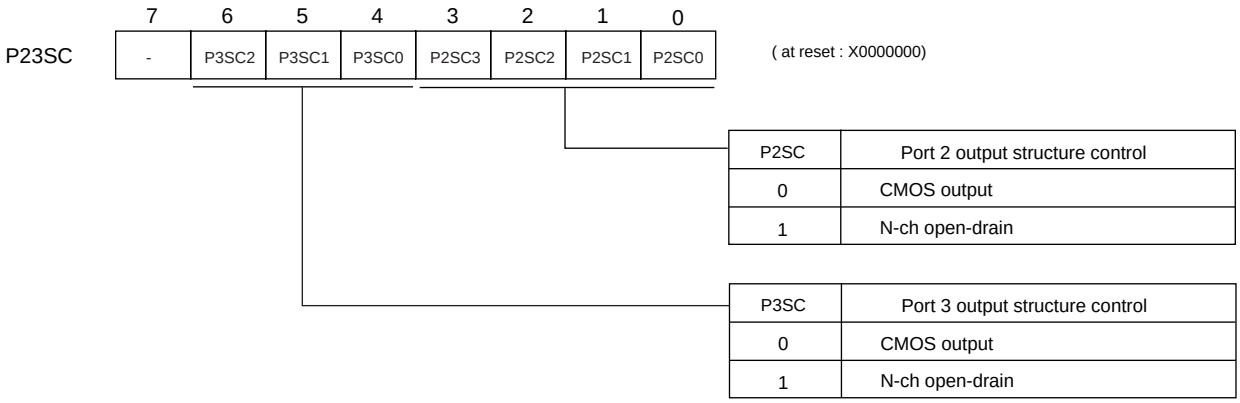


Port 2, Port 3 Direction Control Register (P23DIR : x'012', R/W)



Port 2, Port 3 Pull-up Resistor Control Register (P23PLU : x'022', R/W)

Figure 3-3-1 Port 2, Port 3 Registers (1/2)



Port 2, Port 3 Output Structure Control Register (P23SC : x'02A', R/W)

Figure 3-3-2 Port 2, Port 3 Registers (2/2)

3-3-3 Block Diagram

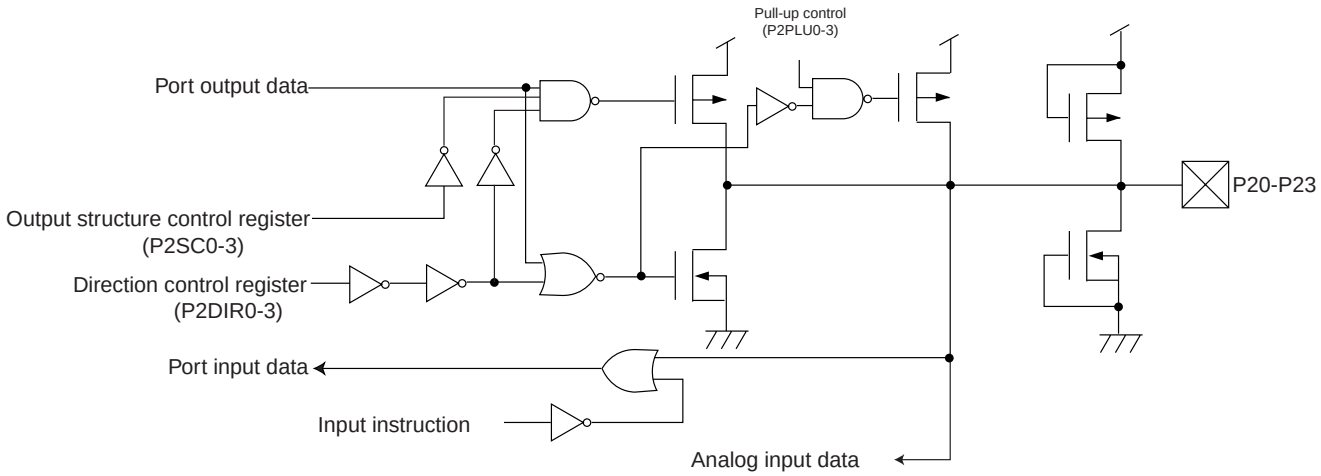


Figure 3-3-3 Block Diagram (P20, P21, P22, P23)

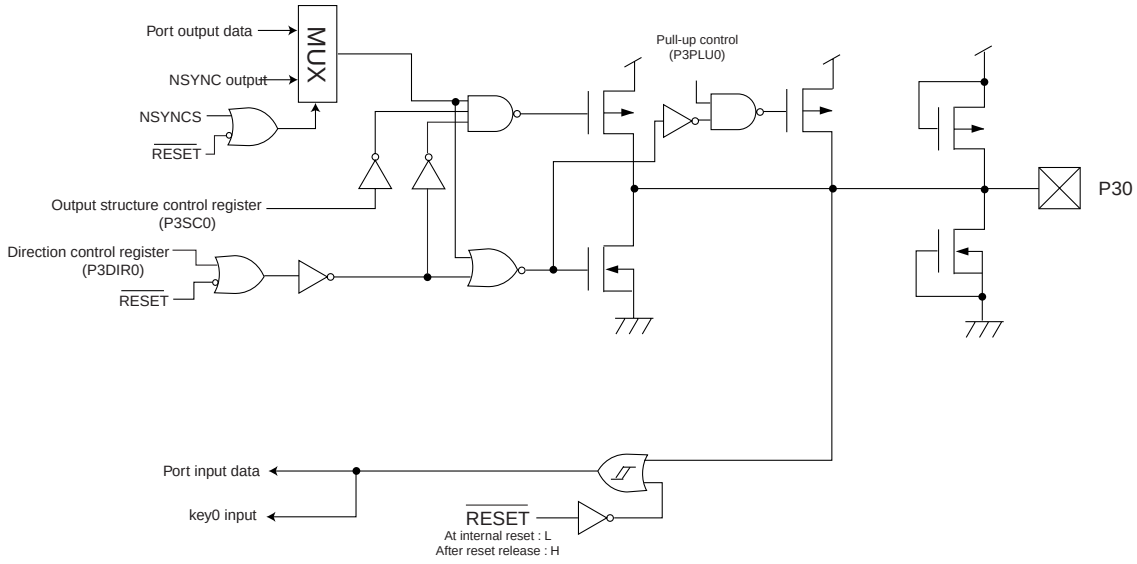


Figure 3-3-4 Block Diagram (P30)

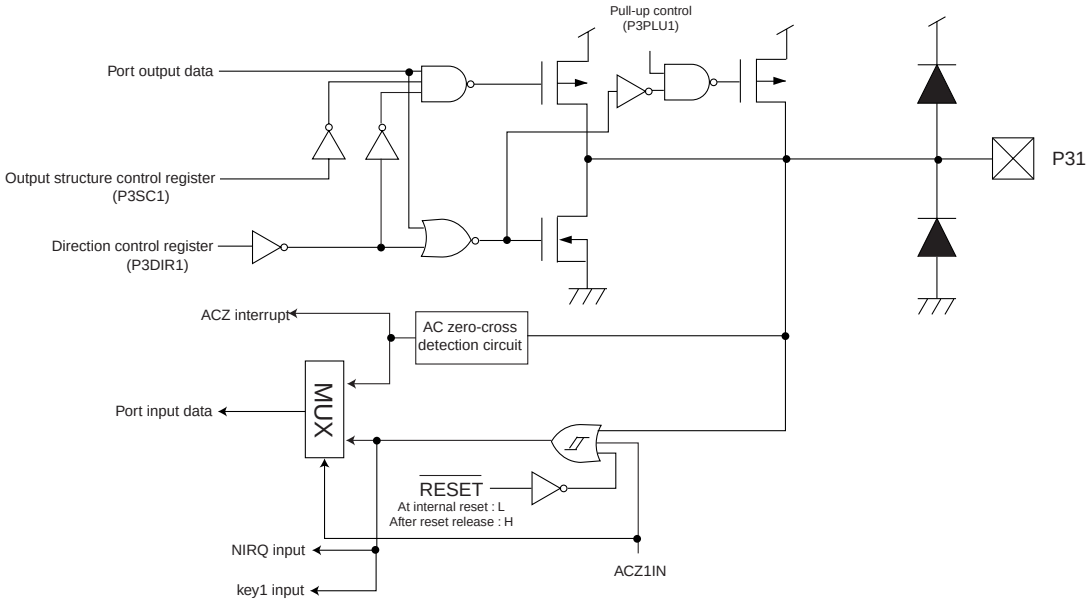


Figure 3-3-5 Block Diagram (P31)

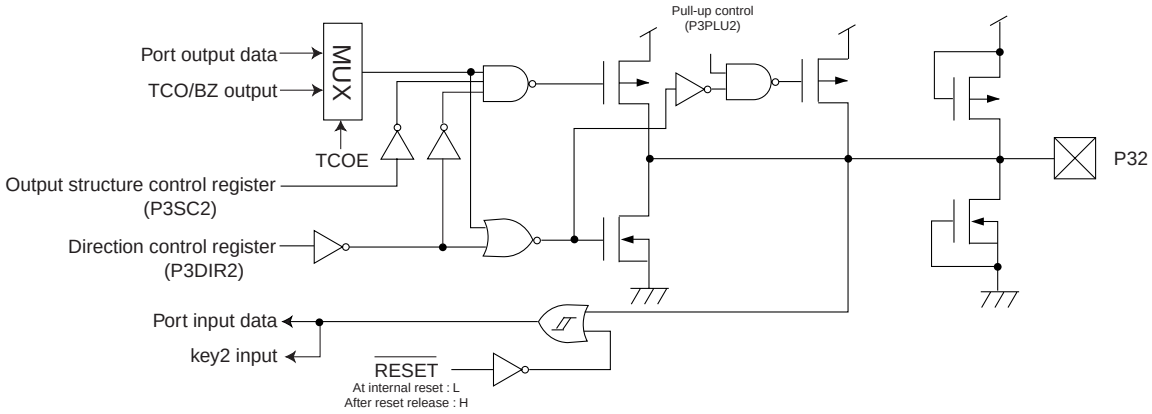


Figure 3-3-6 Block Diagram (P32)

Chapter 4 Interrupts

4-1 Overview

4-1-1 Functions

This LSI has interrupt 1 (IRQ 1), interrupt 2 (IRQ 2) and interrupt 3 (IRQ 3).

Interrupt controller stops the executing program flow by the interrupt request, and, at that time, push program counter (PC) and flag status (FS) to the stack, and controls the execution starting of the interrupt service routine depending on each interrupt factor.

JMP instruction at the starting address can specify the head address of the interrupt service routine.

Table 4-1-1 Interrupt Service Routine Starting Address

Interrupt factor		Vector address
(CPU reset)	(RESET)	x'000'
Interrupt 1	(IRQ1)	x'00A'
Interrupt 2	(IRQ2)	x'00C'
Interrupt 3	(IRQ3)	x'00E'

Priority
High
↕
Low

Interrupt is accepted by the interrupt controller, if only both of the interrupt request flag (IE) and the interrupt enable flag (IF) are set. Once an interrupt is accepted, the interrupt service routine is executed. But other interrupt enable flag is not masked. If multiple interrupts are accepted at the same time, the execution is done in order of priority decided in the hardware. The highest priority is interrupt 1 (IRQ1), then interrupt 2 (IRQ2), then interrupt 3 (IRQ3).

Table 4-1-2 shows the program example of interrupt enable , disable.

Table 4-1-2 Program Example for Interrupt Setup

setup / interrupt	enable	disable
IRQ1	EDI 0,4	EDI 4,0
IRQ2	EDI 0,2	EDI 2,0
IRQ3	EDI 0,1	EDI 1,0

Interrupt request flag (IF) is set to "1" by an interrupt request, and cleared to "0" by the interrupt acceptance. This flag is managed by hardware, but can be reset by software. IRQ mode register (IRQM) can reset the request flag.

Interrupt enable flag (IE) is the flag that enables interrupts in the group. This flag is valid when it is "1".

4-1-2 Block Diagram

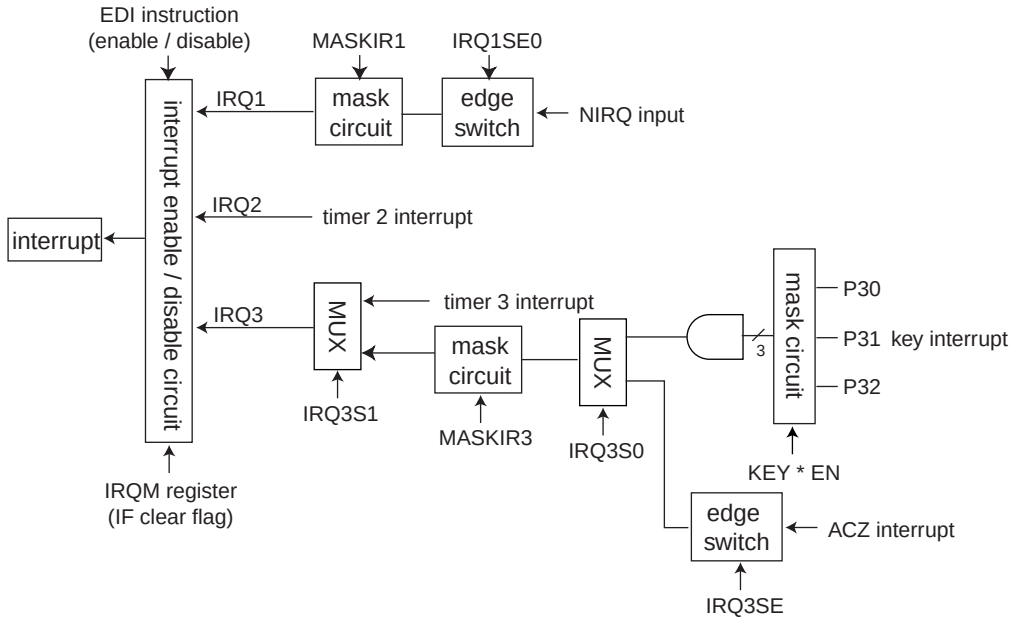


Figure 4-1-1 Interrupt Block Diagram

4-1-3 Operation

■Interrupt Processing Sequence

For interrupts other than reset input, the interrupt processing sequence consists of interrupt request, interrupt acceptance, and hardware processing. After acceptance, the program counter (PC) and the flag status (FS) are saved onto the stack, and execution branches to the starting address specified by the corresponding interrupt vector.

After the interrupt service routine, the program counter and the flag status are restored the contents to the point at which execution was interrupted.

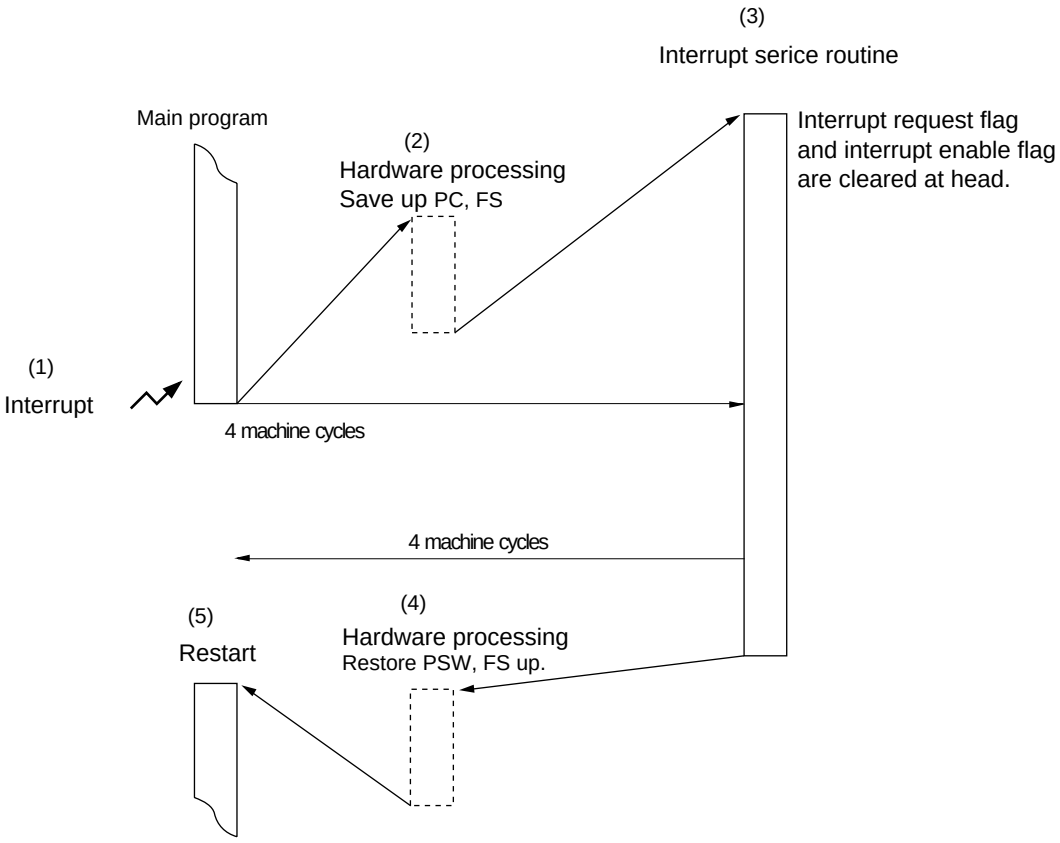


Figure 4-1-2 Interrupt Processing Sequence

■Interrupt Acceptance Operation

The interrupt service routine is started when the interrupt is accepted by branching the program to the head of the interrupt service routine, after an interrupt factor is generated. First of all, if an interrupt factor is generated, the interrupt request flag (IE) with the corresponding level is set. At that time, if the interrupt enable flag is set and it is corresponded to the IF flag, the generated interrupt factor can be accepted.
Acceptance operation is similar to the operation on CALL instruction. On the acceptance cycle, the program counter (PC) and the flag status (FS) are written to the stack. (They are pushed onto the stack.)
Then, the starting address of the interrupt service routine corresponded to the each factor is set to the program counter.
And, reset the IE flag and IF flag, with the corresponded level to the interrupt acceptance.
Each interrupt service routine should be used with JMP instruction at the starting address of the program, if necessary.

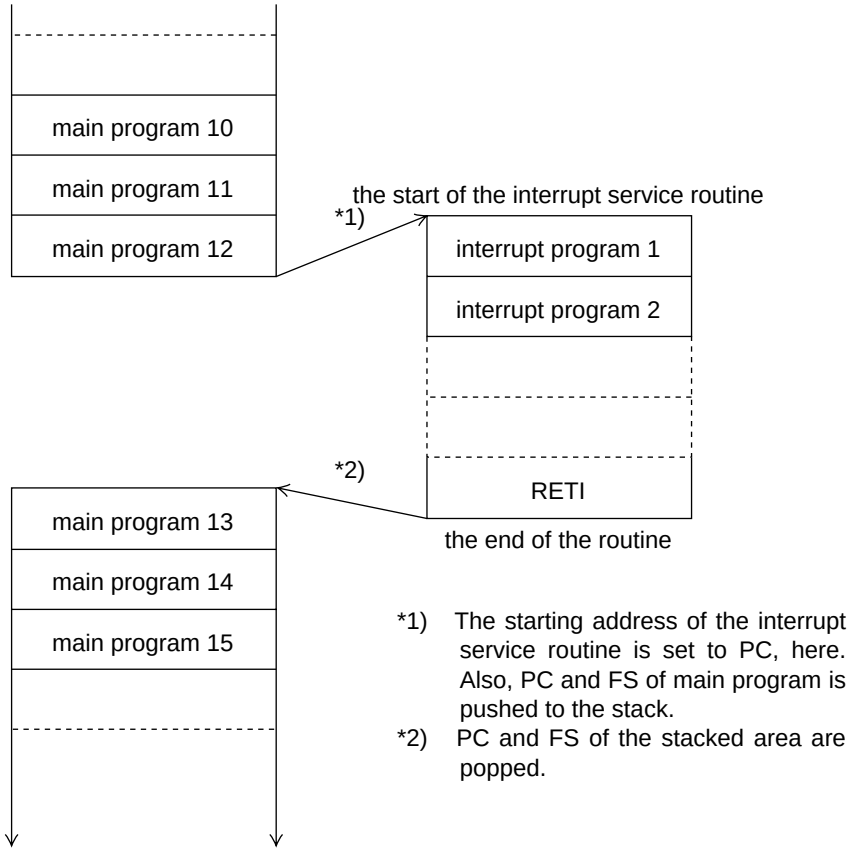


Figure 4-1-3 Interrupt Operation

Figure 4-1-4 Interrupt Sequence Example

■Interrupt return operation

RETI instruction (Return from Interrupt) is used on return operation to the former program. This instruction is similar to the RET instruction (RET) that is used on return operation from subroutine.

RETI instruction return the contents of the program counter (PC) and the flag status (FS), that are pushed onto the stack area (RAM). Then, the program is returned to the status before the interrupt is generated.

For interrupt response speed, it takes 4 cycles after the interrupt factor is generated till the interrupt is accepted. If there is EDI instruction on the head address of the interrupt service routine, 3 to 4 machine cycles interrupt is disabled.

■Stack at interrupt

Stack level at acceptance and at recover are changed as much as the program counter (PC) and the flag status (FS) are pushed or popped.

At normal interrupt, PC and FS are pushed so that 4 nibble of the stack area (RAM) is needed. Therefore, the value of SP is on the decrement for 4 at acceptance and on the increment for 4 at recover.

Recover operation is done by RETI instruction. RETI instruction restore the contents of FS, PC that are pushed onto the stack area (RAM) and the exclusive stack area on the acceptance cycle. After the value of the stack area that SP indicates are read out, SP is on the increment.

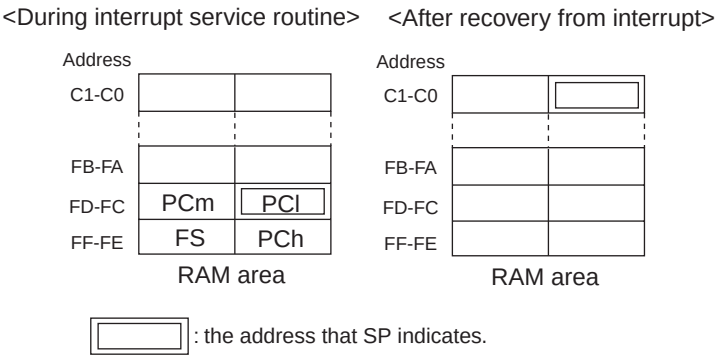


Figure 4-1-5 Operation of Stack Pointer

■Interrupt Acceptance, Start and Finish

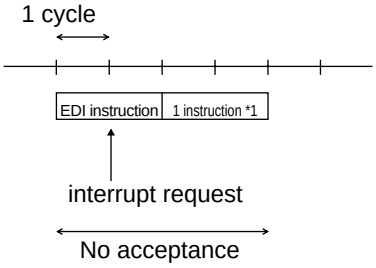
The interrupt acceptance is not available at the following timing.

(1) During interrupt is disabled.

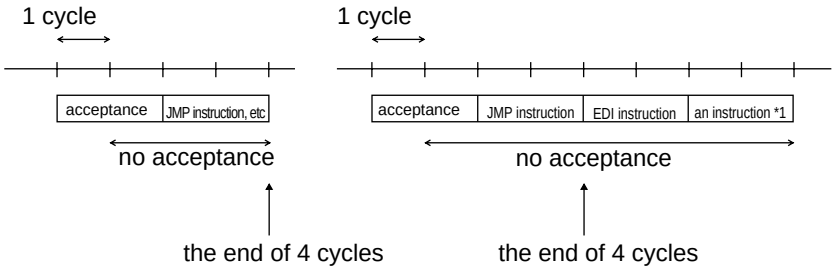
(2) At the 1st cycle of 2 cycles instruction.

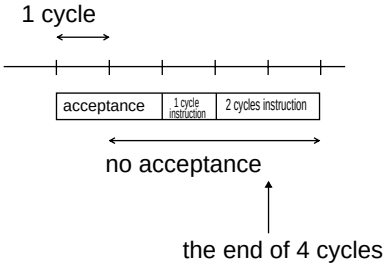
(3) At the 1st, 2nd cycle of 3 cycles instruction.

(4) When the interrupt factor is generated in execution of EDI instruction, interrupt acceptance is disabled till the next instruction is completed.



(5) The interrupt acceptance is disabled after the interrupt is accepted till 4 cycles are completed. Also, if EDI instruction comes after that, the acceptance is disabled till EDI instruction and the next instruction are completed.

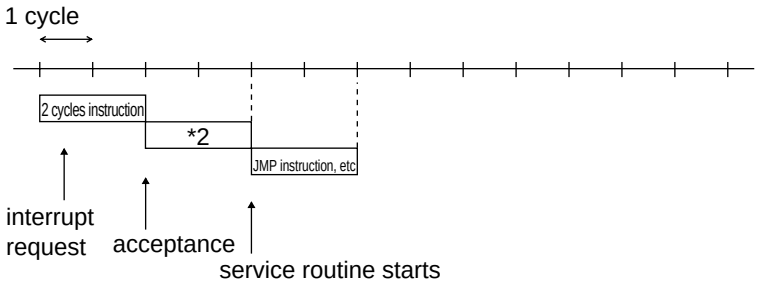




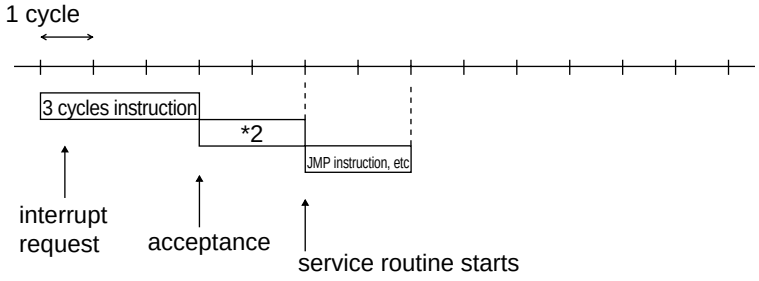
*1 At 1 cycle instruction, the acceptance is disabled till 1 cycle instruction is completed.
At 2 cycles instruction, the acceptance is disabled till 2 cycles instruction is completed.
At 3 cycles instruction, the acceptance is disabled till 3 cycles instruction is completed.

Here is the example for acceptance operation.

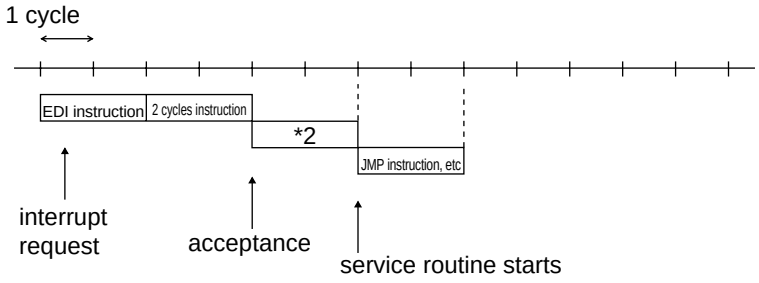
- When the interrupt factor is generated in execution of 2 cycles instruction, the interrupt acceptance is started after 2 cycles instruction is completed.



- When the interrupt factor is generated in execution of 3 cycles instruction, the interrupt acceptance is started after 3 cycles instruction is completed.



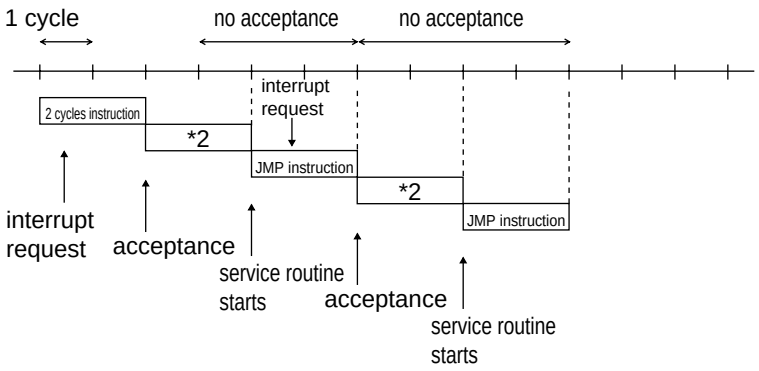
- When the interrupt factor is generated in execution of EDI instruction and the next instruction (1, 2, or 3 cycles instruction), the interrupt acceptance is started after the instruction (max. 5 cycles) is completed.



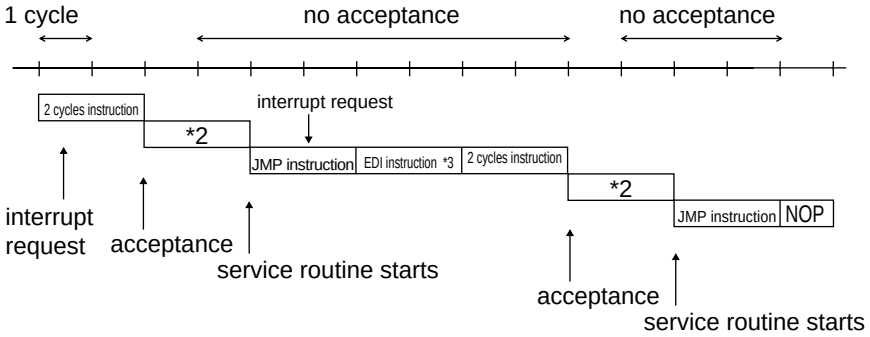
*2 1. The contents of PC and FS in main program are pushed to the stack area.
2. The starting address of the interrupt service routine is set to PC.
3. IF and IE of the accepted interrupt are reset.

■Interrupt Acceptance, Start and Finish (at multiple interrupts)
Here is the example of acceptance at multiple interrupts.

❍When the interrupt factor is generated in execution of instruction at the beginning of the interrupt service routine, the interrupt acceptance is started after the instruction is completed (except when the next instruction to JMP instruction is EDI instruction.).



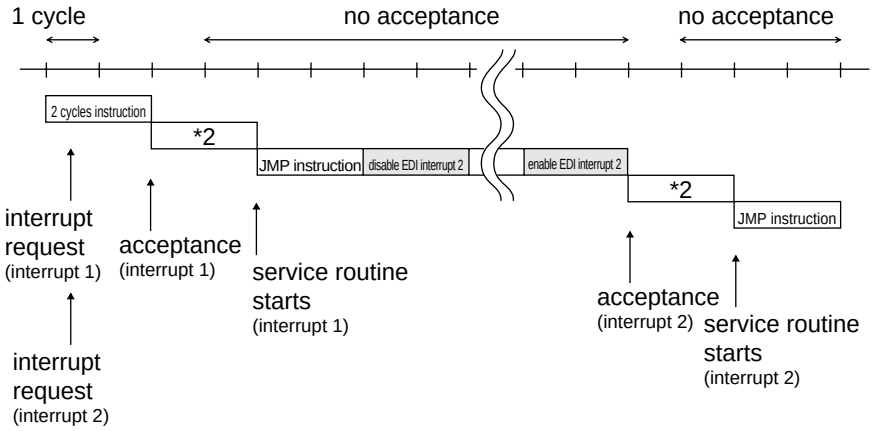
❍When the interrupt factor is generated in execution of instruction at the beginning of the interrupt service routine (Instructions is JMP + EDI), the interrupt acceptance is started after the next instruction to EDI is completed.



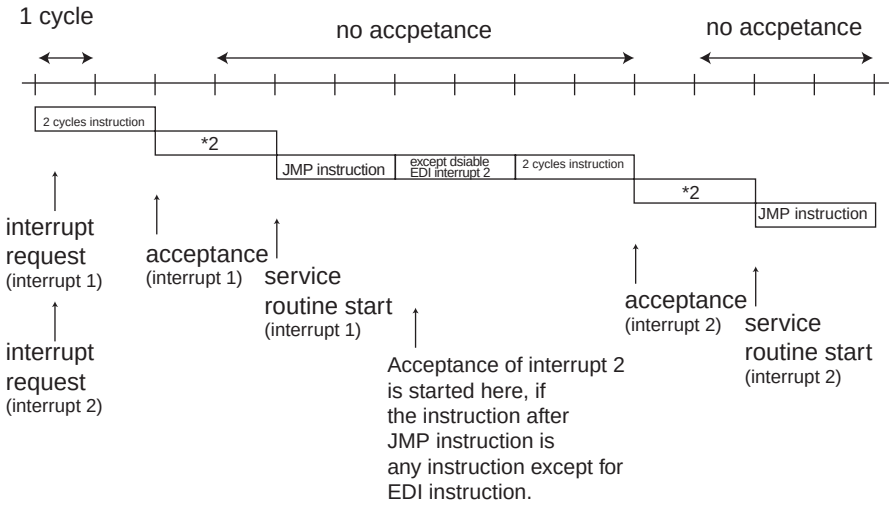
*2 1. The contents of PC and FS in main program are pushed to the stack area.
2. The starting address of the interrupt service routine is set to PC.
3. IF and IE of the accepted interrupt are reset.

*3 EDI instruction that does not disable an interrupt.

❍When two interrupt factors are generated at the same time, the interrupt with higher priority is accepted.



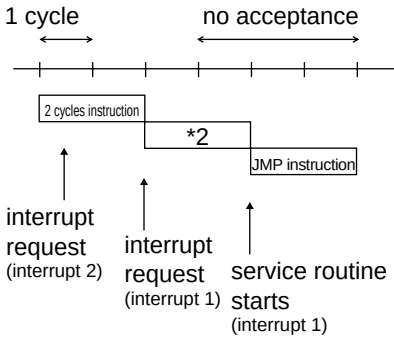
❍When two interrupt factors are generated at the same time, the interrupt with higher priority is accepted. If the second interrupt is not disabled in the program, the operation is switched to accept the second one.



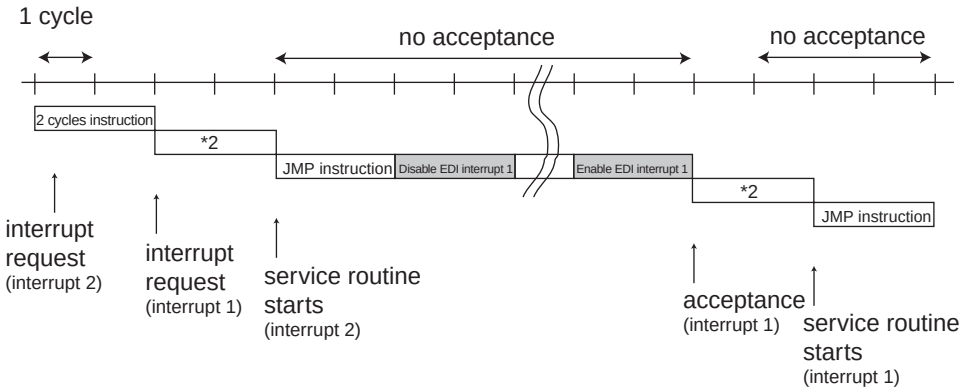
*2 1. The contents of PC and FS in main program are pushed to the stack area.
2. The starting address of the interrupt service routine is set to PC.
3. IF and IE of the accepted interrupt are reset.

This example shows the case when the interrupt 2 is not disabled after the interrupt with higher priority (the interrupt 1) is accepted first. Therefore, during the service routine of the interrupt 1, only 3 instructions (JMP, EDI, 2 cycles instruction) are executed, then the operation is switched to the acceptance of the interrupt 2.

- When an interrupt factor with high priority is generated at the acceptance operation (at 1st cycle), it is regarded as a multiple interrupt, and the interrupt with higher priority is accepted.



- When an interrupt factor with high priority is generated at the acceptance operation (at 2nd cycle), the first interrupt is accepted.



*2 1. The contents of PC and FS in main program are pushed to the stack area.
2. The starting address of the interrupt service routine is set to PC.
3. IF and IE of the accepted interrupt are reset.

4-1-4 Setup Example

■NIRQ External Interrupt Setup Example

P31 / NIRQ pin is input pulse, and interrupt 1 (IRQ1) is generated at the falling edge.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the pin. P23DIR (x'012') bp5 :P3DIR1 = 0	(1) Set the P3DIR1 flag of the port 2, port 3 direction control register (P23DIR) to "0" for P31 /NIRQ to set to input mode. If necessary, add pull-up resistor. [☞ Chapter 3. Ports]
(2) Select the interrupt source. IRQC0 (x'034') bp4 :IRQ1S0 = 0	(2) Select interrupt 1 as the interrupt source by the IRQ1S0 flag of the interrupt control register 0 (IRQC0).
(3) Select the interrupt edge. IRQC0 (x'034') bp6 :IRQ1SE0 = 0	(3) Set the lRQ1SE0 flag of the interrupt control register 0 (IRQC0) to "0" to select the interrupt edge to the falling edge.
(4) Enable the interrupt edge. IRQC0 (x'034') bp7 :MASKIR1 = 1	(4) Enable the interrupt edge by the MASKIR1 flag of the interrupt control register 0 (IRQC0).
(5) Clear the interrupt request flag. IRQM (x'032') bp5 :IFIRQ1E = 1	(5) Set the IFIRQ1E flag of the IRQ mode register (IRQM) to "1" to clear the interrupt 1 request flag.
(6) Enable the interrupt 1.	(6) Execute EDI instruction to enable interrupt 1.

■Key Interrupt setup procedure (P30, P31, P32)

P30 / key 0 is input pulse to generate at the falling edge.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the pin. P23DIR (x'012') bp5 : P3DIR0 = 0	(1) Set the P3DIR0 flag of the port 2, port 3 direction control register (P23DIR) to "0" for P30 / key 0 to set to input mode. If necessary, add pull-up resistor. [☞ Chapter 3. Ports]
(2) Select the interrupt source. KEYCNT (x'038') bp4 : KEY0EN = 1 IRQC1 (x'036') bp1-0 : IRQ3S1-0 = 00 bp2 : IRQ3SE = 0 bp3 : MASKIR3 = 1	(2) Set the KEY0EN flag of the key interrupt control register 1 (KEYCNT) to "1" to select the key interrupt (key 0) as the interrupt source by the interrupt control register 1 (IRQC1) register.
(3) Clear the interrupt request flag. IRQM (x'032') bp7 : IFIRQ3E = 1	(3) Set the IFIRQ3E flag of the IRQ mode register (IRQM) to "1" to clear the interrupt 3 request flag.
(4) Enable the interrupt 3.	(4) Execute EDI instruction to enable interrupt 3.

4-2 Control Registers

4-2-1 Registers List

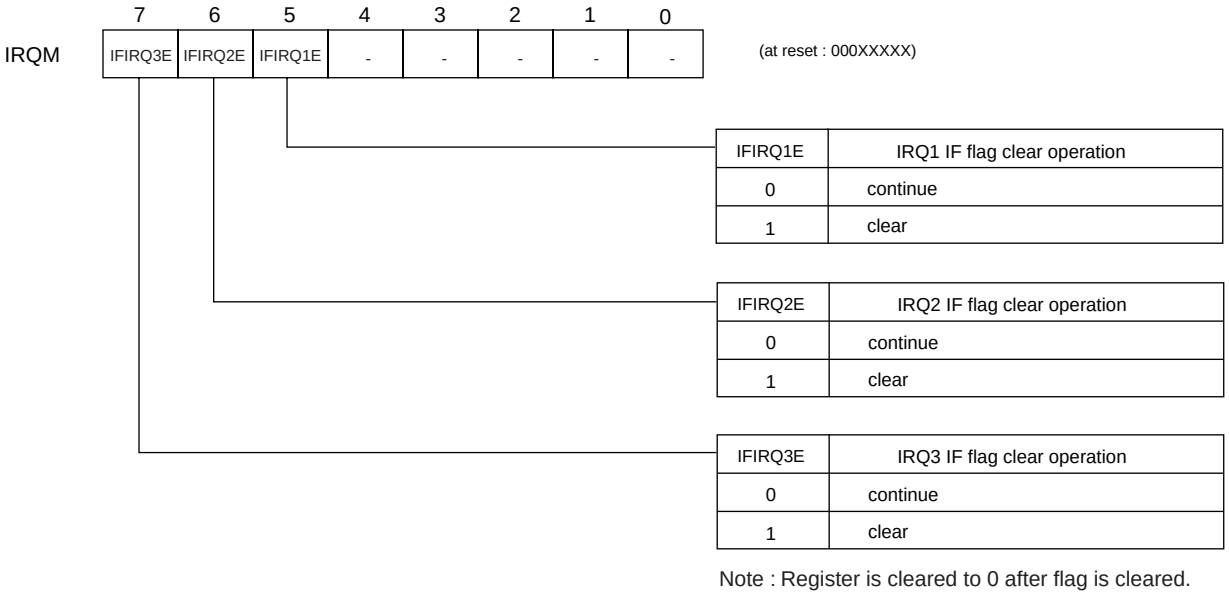
There are 4 registers to control interrupt operation, the IRQ mode register (IRQM), the interrupt control register 0 (IRQC0), the interrupt control register 1 (IRQC1) and the key interrupt control register 1 (KEYCNT).

Table 4-2-1 Interrupt Control Registers

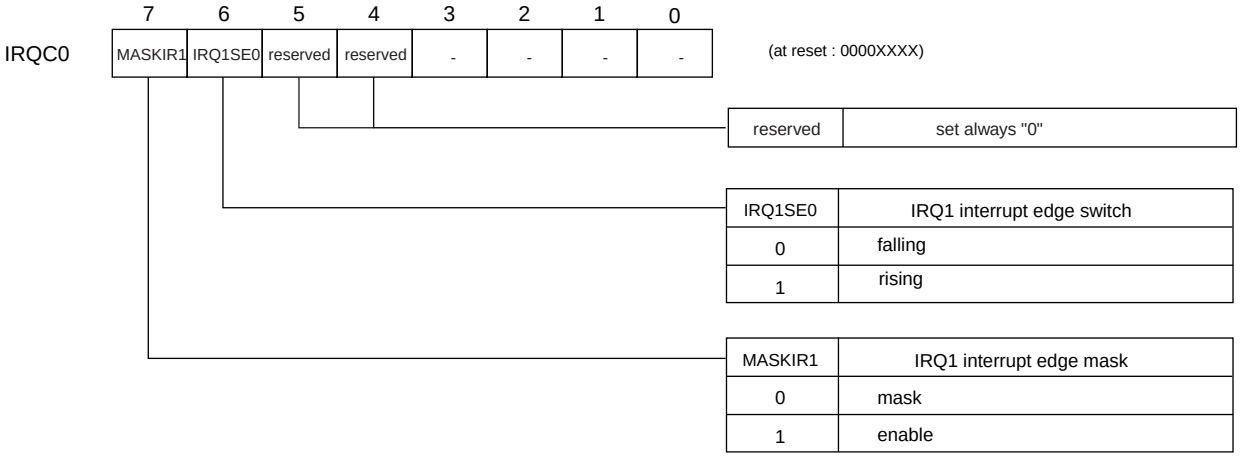
Register	Address	R/W	Function	Page
IRQM	x'032'	W	IRQ mode register	IV - 16
IRQC0	x'034'	R/W	Interrupt control register 0	IV - 16
IRQC1	x'036'	R/W	Interrupt control register 1	IV - 17
KEYCNT	x'038'	R/W	Key interrupt control register 1	IV - 17

R / W : Readable / Writable
W : Writable only

4-2-2 Interrupt Control Registers

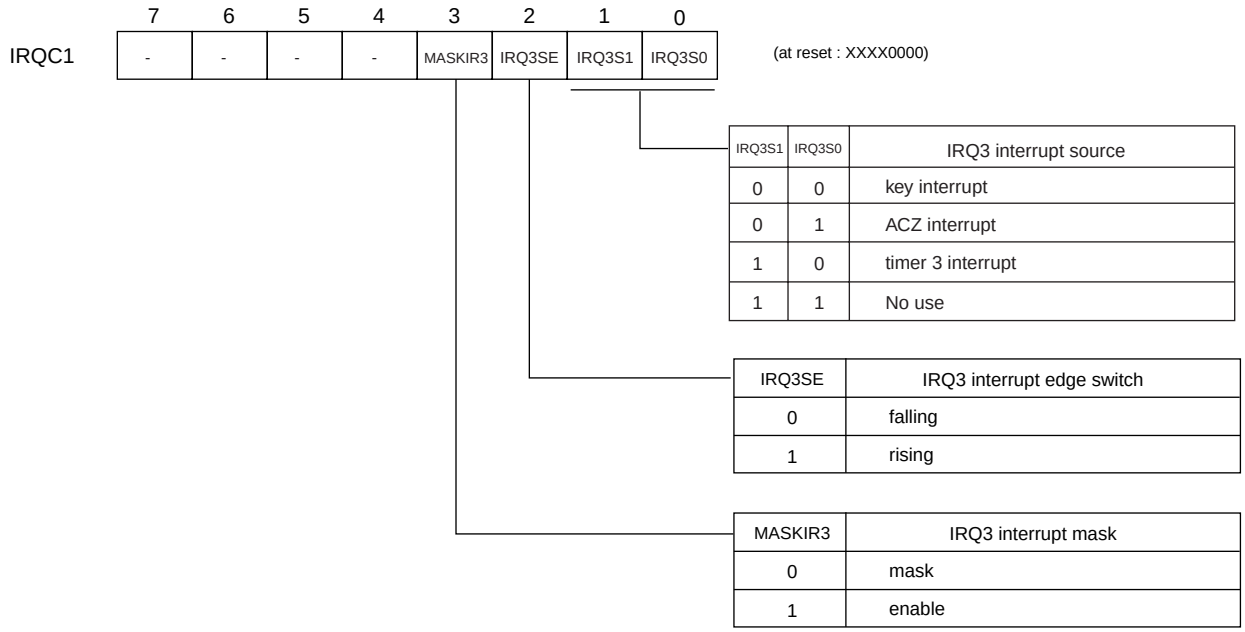


IRQ Mode Register (IRQM : x'032', W)

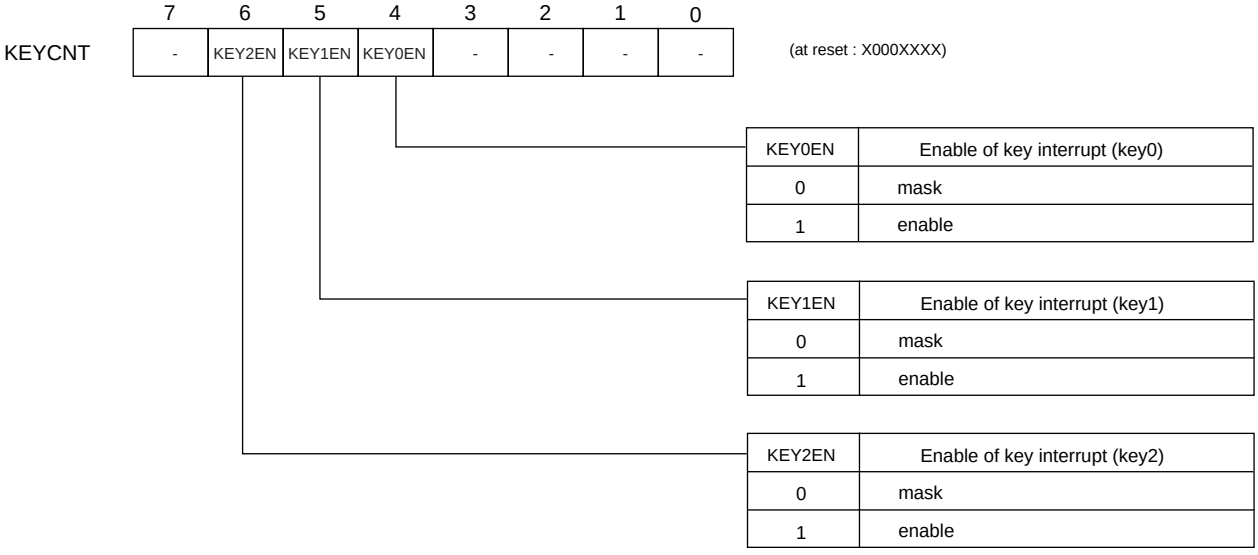


Interrupt Control Register 0 (IRQC0 : x'034', R/W)

Figure 4-2-1 Interrupt Control Register (1/2)



Interrupt Control Register 1 (IRQC1 : x'036', R/W)



Key Interrupt Control Register 1 (KEYCNT : x'038', R/W)

Figure 4-2-2 Interrupt Control Register (2/2)

Chapter 5 Timer

5

5-1 8-Bit Timer

This LSI contains two general 8-bit timers (Timer 2, Timer 3). The general 8-bit timers can be used as a 16-bit timer on cascade connection.

Fosc or fsys can be selected as clock source of each timer, by using output from prescaler. Also, remote control output circuit is built in.

P32 / TCO pin can output pulse signal for each timer. At output to P32 / TCO pin, set output mode by the port 2, port 3 direction control register (P23DIR), and select the timer 3 output by the timer output control register (TCOCNT x'06A'). At output to P10/PWMO0-P13/PWMO3 pin, set output mode by the port 0, port 1 direction control register (P01DIR), and set the port 0, port 1 data register (PORT01) to "1" to output "H". Select PWM output by the buzzer output control register (BZCTR x'06C').

5-1-1 Functions

Table 5-1-1 shows functions that can be used with each timer.

Table 5-1-1 Timer Functions

		timer 2 (8 bit)	timer 3 (8 bit)
independent	interrupt factor	interrupt 2 (IRQ2)	interrupt 3 (IRQ3)
	8-bit timer operation	√	√
	timer pulse output	√	√
	remote control carrier output	√	√
	PWM output	√	-
cascade connection	interrupt factor	interrupt 3(IRQ3)	
	16-bit timer operation	√	
	timer pulse output	√	
	high precision PWM output	√	
clock source		fsys/2 fsys/8 fsys/32 fsys/128 fosc fosc/4 fosc/16 fosc/64	fsys/2 fosc fosc/2^6 fosc/2^{14}
fosc : machine clock (oscillation input) fsys : system clock [☞ Chapter 2. 2-4 Clock Switching]			
ohter		built-in prescaler (7 steps)	

5-1-2 Block Diagram

■Timer 2 Block Diagram

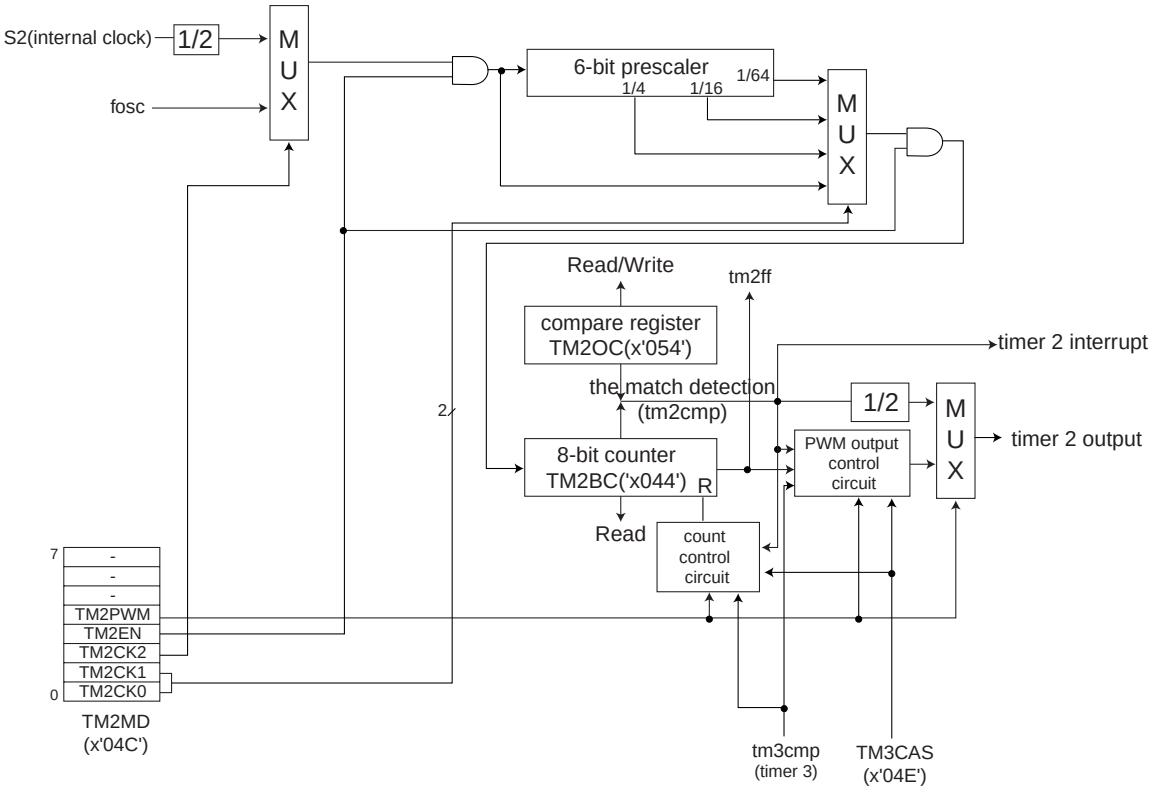


Figure 5-1-1 Timer 2 Block Diagram

■Timer 3 Block Diagram

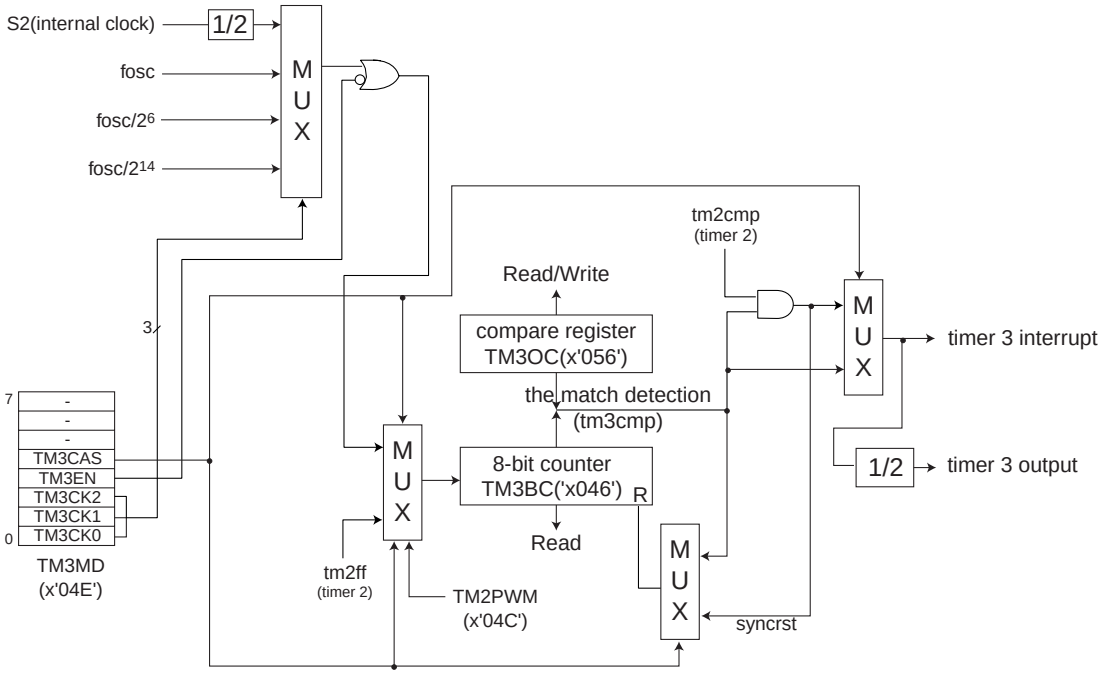


Figure 5-1-2 Timer 3 Block Diagram

■Timer Output Block Diagram

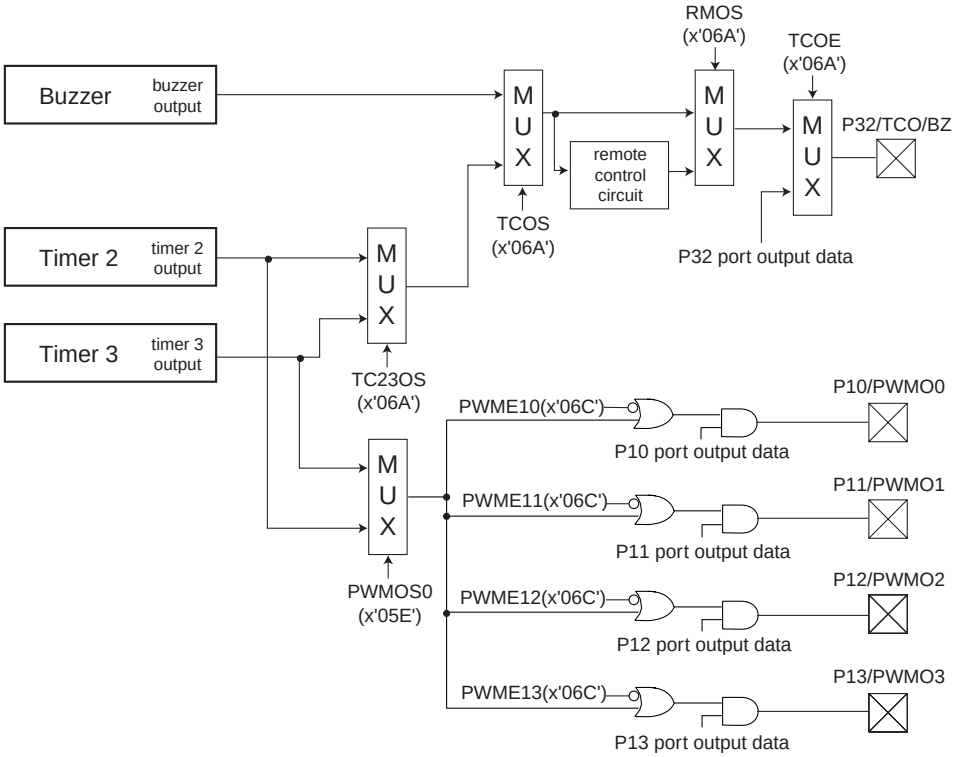


Figure 5-1-3 Timer Output Block Diagram

■Remote Control Circuit Block Diagram

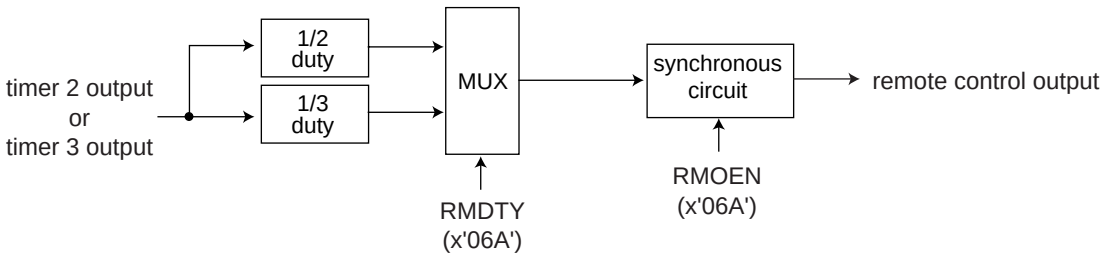


Figure 5-1-4 Remote Control Output Block Diagram

■Buzzer Output Block Diagram

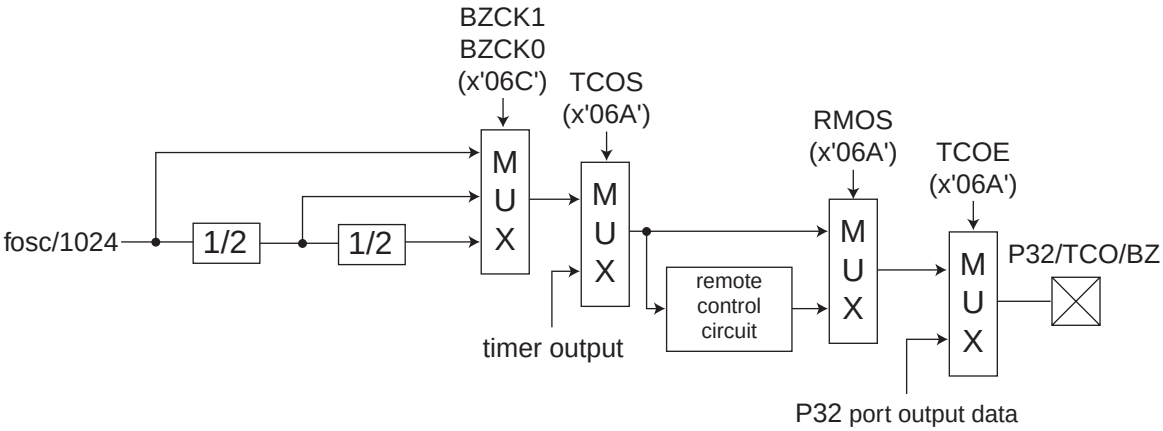


Figure 5-1-5 Buzzer Output Block Diagram

5-2 8-Bit Timer Control Registers

Each of timer 2 and timer 3 consists of the binary counter (TMnBC) and the compare register (TMnOC). And they are controlled by the mode register (TMnMD).

5-2-1 Registers

Table 5-2-1 8-bit Timer Control Registers

	register	address	R/W	function	page
timer 2	TM2BC	x'044'	R	timer 2 binary counter	V - 10
	TM2OC	x'054'	R/W	timer 2 compare register	V - 9
	TM2MD	x'04C'	R/W	timer 2 mode register	V - 11
	MODCNT	x'05E'	R/W	timer mode control register	V - 12
	TCOCNT	x'06A'	R/W	timer output control register	V - 13
	P01DIR	x'010'	R/W	port 0, port 1 direction control register	Ⅲ - 9
	P23DIR	x'012'	R/W	port 2, port 3 direction control register	Ⅲ - 13
	BZCTR	x'06C'	R/W	buzzer output control register	V - 14
timer 3	TM3BC	x'046'	R	timer 3 binary counter	V - 10
	TM3OC	x'056'	R/W	timer 3 compare register	V - 9
	TM3MD	x'04E'	R/W	timer 3 mode register	V - 12
	TCOCNT	x'06A'	R/W	timer output control register	V - 13
	P01DIR	x'010'	R/W	port 0, port 1 direction control register	Ⅲ - 9
	P23DIR	x'012'	R/W	port 2, port 3 direction control register	Ⅲ - 13
	BZCTR	x'06C'	R/W	buzzer output control register	V - 14

R/W : Readable / Writable
R : Readable only

5-2-2 Compare Registers

Compare register is register that the value compared to the binary counter is set.

■Timer 2 Compare Register (TM2OC)

	7	6	5	4	3	2	1	0	
TM2OC	TM2OC7	TM2OC6	TM2OC5	TM2OC4	TM2OC3	TM2OC2	TM2OC1	TM2OC0	(at reset : X X X X X X X X)

Timer 2 Compare Register (TM2OC : x'054', R/W)

■Timer 3 Compare Register (TM3OC)

	7	6	5	4	3	2	1	0	
TM3OC	TM3OC7	TM3OC6	TM3OC5	TM3OC4	TM3OC3	TM3OC2	TM3OC1	TM3OC0	(at reset : X X X X X X X X)

Timer 3 Compare Register (TM3OC : x'056', R/W)

Figure 5-2-1 Compare Register

5-2-3 Binary Counters

Binary counter is 8-bit up counter. Binary counter is cleared to x'00', if any data is written to this counter during counting is stopped.

■Timer 2 Binary Counter (TM2BC)

	7	6	5	4	3	2	1	0	
TM2BC	TM2BC7	TM2BC6	TM2BC5	TM2BC4	TM2BC3	TM2BC2	TM2BC1	TM2BC0	(at reset : X X X X X X X X)

Timer 2 Binary Counter (TM2BC : x'044', R)

■Timer 3 Binary Counter (TM3BC)

	7	6	5	4	3	2	1	0	
TM3BC	TM3BC7	TM3BC6	TM3BC5	TM3BC4	TM3BC3	TM3BC2	TM3BC1	TM3BC0	(at reset : X X X X X X X X)

Timer 3 Binary Counter (TM3BC : x'046', R)

Figure 5-2-2 Binary Counter

5-2-4 Timer Control Registers

■Timer 2 Mode Register (TM2MD)

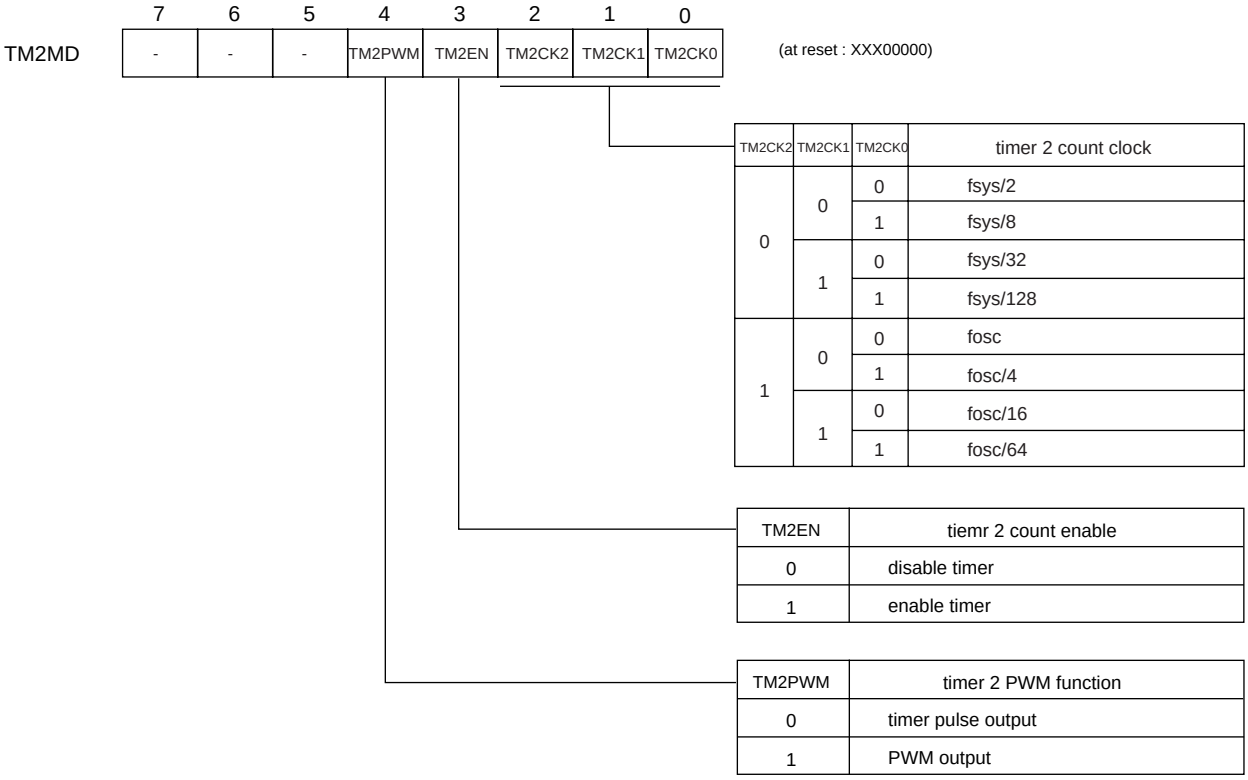
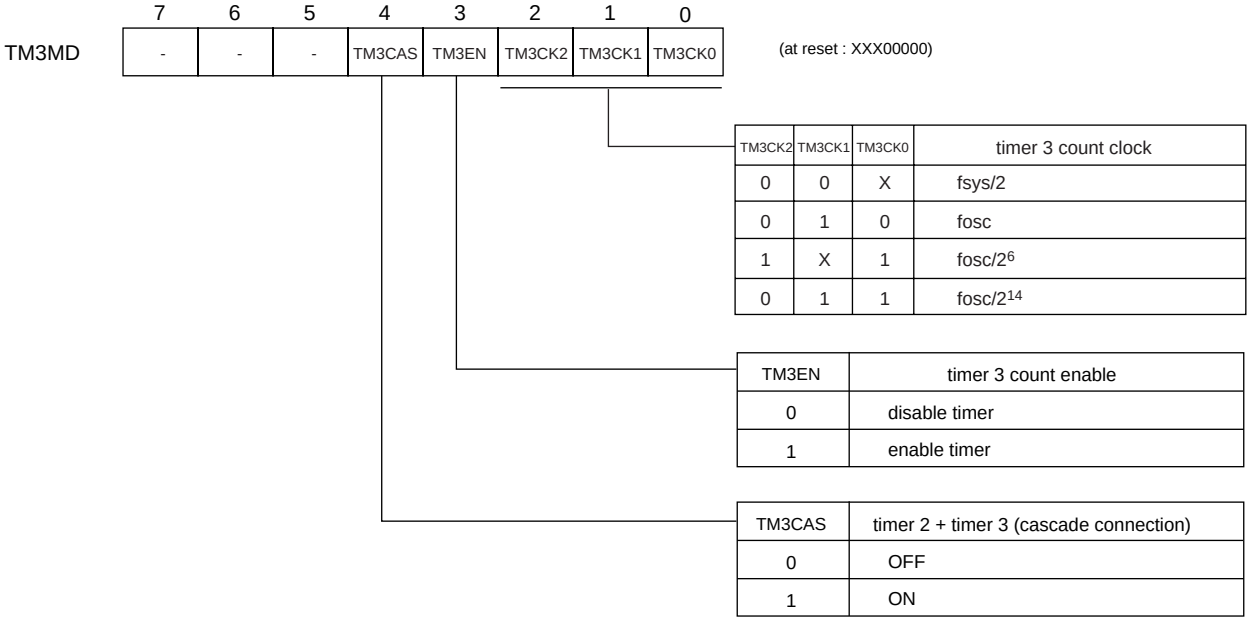


Figure 5-2-3 Timer 2 Mode Register (TM2MD : x'04C', R/W)

■Timer 3 Mode Register (TM3MD)



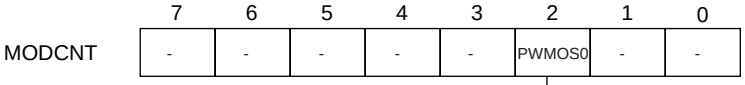
TM3CK2	TM3CK1	TM3CK0	timer 3 count clock
0	0	X	fsys/2
0	1	0	fosc
1	X	1	$fosc/2^6$
0	1	1	$fosc/2^{14}$

TM3EN	timer 3 count enable
0	disable timer
1	enable timer

TM3CAS	timer 2 + timer 3 (cascade connection)
0	OFF
1	ON

Figure 5-2-4 Timer 3 Mode Register (TM3MD : x'04E', R/W)

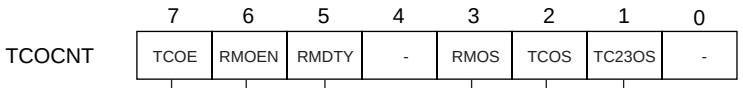
■Timer Mode Control Register (MODCNT)



PWMOS0	timer output
0	timer 2 output
1	timer 3 output

Figure 5-2-5 Timer Mode Control Register (MODCNT : x'05E', R/W)

■Timer Output Control Register (TCOCNT)



TC23OS	timer 2, timer 3 output
0	timer 2
1	timer 3

TCOS	timer output , buzzer output
0	buzzer output
1	timer 2, timer 3 output

RMOS	TCO output
0	timer output
1	remote control output

RMDTY	remote control output duty
0	1/2 duty
1	1/3 duty

RMOEN	remote control output enable
0	output low level
1	output carrier

TCOE	timer output enable
0	port output data
1	TCO

TCOE	RMOS	TCOS	TC23OS	P32/TCO/BZ output
1	0	0	X	buzzer output
1	0	1	0	timer 2 output
1	0	1	1	timer 3 output
X	1	0	X	unused
1	1	1	0	remote control output (base cycle is timer 2 output)
1	1	1	1	remote control output (base cycle is timer 3 output)
0	X	X	X	P32 port data output

Figure 5-2-6 Timer Output Control Register (TCOCNT : x'06A', R/W)

■Buzzer Output Control Register (BZCTR)

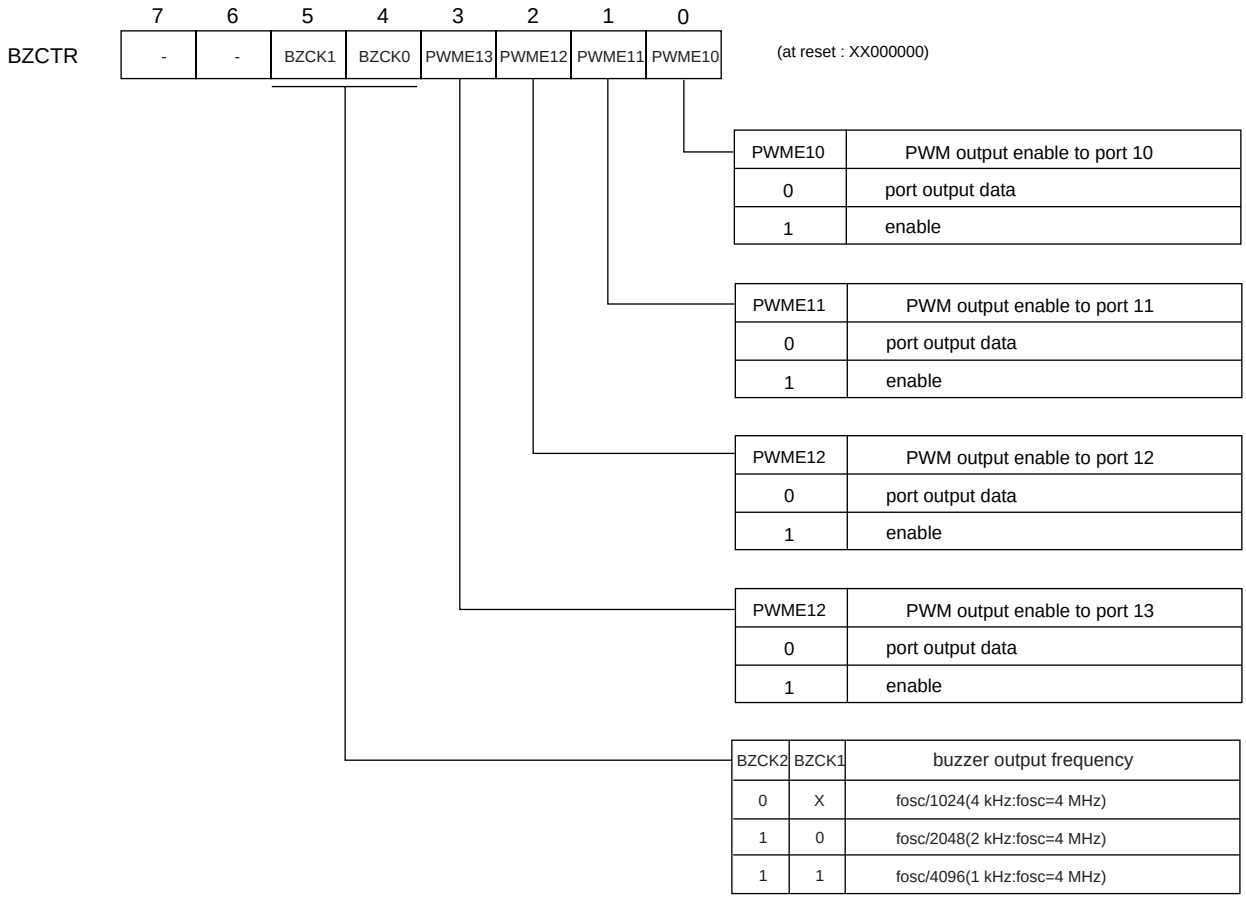


Figure 5-2-7 Buzzer Output Control Register (BZCTR : x'06C', R/W)

5-3 8-Bit Timer Operation

5-3-1 Operation

The timer operation can constantly generate interrupts.

■8-Bit Timer Operation (Timer 2, Timer 3)
The generation cycle of timer interrupts is set by the clock source selection and the setting value of the compare register (TMnOC), in advance. If the binary counter (TMnBC) reaches the setting value of the compare register, an interrupt request is generated at the next count clock, then binary counter is cleared and counting up is restarted from x'00'.
Table 5-3-1 shows clock source that can be selected by timer.

Table 5-3-1 Clock Source (Timer 2, Timer 3) at Timer Operation

clcok source	timer 2 (8 bit)	timer 3 (8 bit)
fosc	√	√
fosc/2	-	-
fosc/4	√	-
fosc/16	√	-
fosc/64(2^6)	√	√
fosc/2^{14}	-	√
fsys/2	√	√
fsys/8	√	-
fsys/32	√	-
fsys/128	√	-

■Count Timing of Timer Operation (Timer 2, Timer 3)

Binary counter counts up with selected clock source as a count clock.

The basic operation of the whole function of 8-bit timer is as follows ;

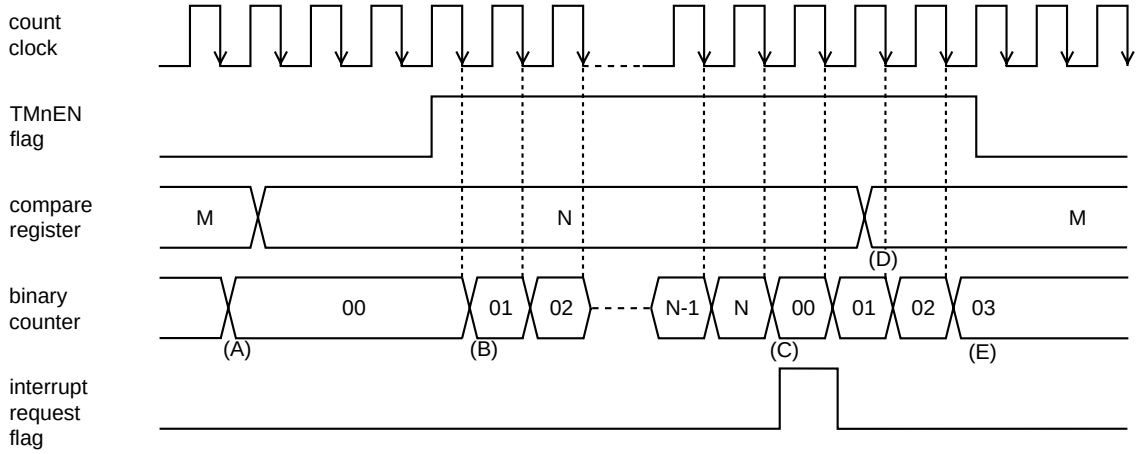


Figure 5-3-1 Count Timing of Timer Operation (Timer 2, Timer 3)

(A) If the value is written to the compare register during the TMnEN flag is stopped ("0"), the binary counter is cleared to x'00', at the writing cycle.

(B) If the TMnEN flag is operated ("1"), the binary counter is started to count.
The counter starts to count up at the falling edge of the count clock.

(C) If the binary counter reaches the value of the compare register, the interrupt request flag is set at the next count clock, then the binary counter is cleared to x'00' and the counting is restarted.

(D) Even if the compare register is rewritten during the TMnEN flag is enabled ("1"), the binary counter is not changed.

(E) If the TMnEN flag is stopped ("0"), the binary counter is stopped.

If the binary counter reaches the value of the compare register, the interrupt request flag is set at the next count clock, then the binary counter is cleared. So, set as follows ;
(the setting value of the compare register) = (the count till the interrupt request is generated - 1)

If the compare register is set the smaller than the binary counter during the count operation, the binary counter counts up till the overflow.

If the interrupt is used, the timer interrupt request flag should be cleared before timer is started.

The timer n interrupt request generation (at TMnOC = x'00') has the same waveform at TMnOC = x'01'.

5-3-2 Setup Example

■Timer Operation Setup Example (Timer 2, Timer 3)

Timer 2 can generate the constant interrupt. Interrupt is generated in every 250 counts by selecting fsys/8 as a clock source.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM2MD (x'04C') bp3 : TM2EN = 0	(1) Set the TM2EN flag of the timer 2 mode register (TM2MD) to "0" to stop the counting of timer 2.
(2) Select the normal timer operation. TM2MD (x'04C') bp4 : TM2PWM = 0	(2) Set the TM2PWM flag of the TM2MD register to "0" to select the normal timer operation.
(3) Select the count clock source. TM2MD (x'04C') bp2-0 : TM2CK2-0 = 001	(3) Set the TM2CK2-0 flag of the TM2MD register to "001" to select fsys/8 as a clock source.
(4) Set the generation cycle. TM2OC (x'054') = x'F9'	(4) Set the interrupt generation cycle to the timer 2 compare register (TM2OC). It is divided by 250, so set the value to 249 (x'F9'). At that time, the timer 2 binary counter (TM2BC) is cleared to x'00'.
(5) Clear the interrupt request flag. IRQM (x'032') bp5 : IFIRQ2E = 1	(5) Set the IFIRQ2E flag of the IRQ mode register (IRQM) to "1" to clear the interrupt 2 request flag.
(6) Enable the interrupt.	(6) Execute EDI instruction to enable interrupt 2. [☞ Chapter 4. Interrupts 4-1-1.].
(7) Start the timer. TM2MD (x'04C') bp3 : TM2EN = 1	(7) Set the TM2EN flag of the TM2MD register to "1" to start the timer 2.

The TM2BC starts to count up from 'x00'. When the TM2BC reaches the setting value of the TM2OC register, the interrupt 2 request flag is set at the next count clock, then the value of the TM2BC becomes x'00' and restart to count up.

When the TMnEN flag of the TMnMD register is changed at the same time to other bit, binary counter may start to count up by the switching operation.

5-4 8-Bit Timer Pulse Output

5-4-1 Operation

TCO or port 1 can output pulse signal with arbitrary frequency.

■Timer Pulse Output Operation (timer 2, timer 3)
The output signal has the twice cycle to the set value in the compare register (TMnOC). Table 5-4-1 shows output pins.

Table 5-4-1 Event Count Input Clock

	timer 2	timer 3
pulse output pin	TCO output(P32) P10-P13 pins	TCO output(P32) P10-P13 pins

■Count Timing of Timer Pulse Output (Timer 2, Timer 3)

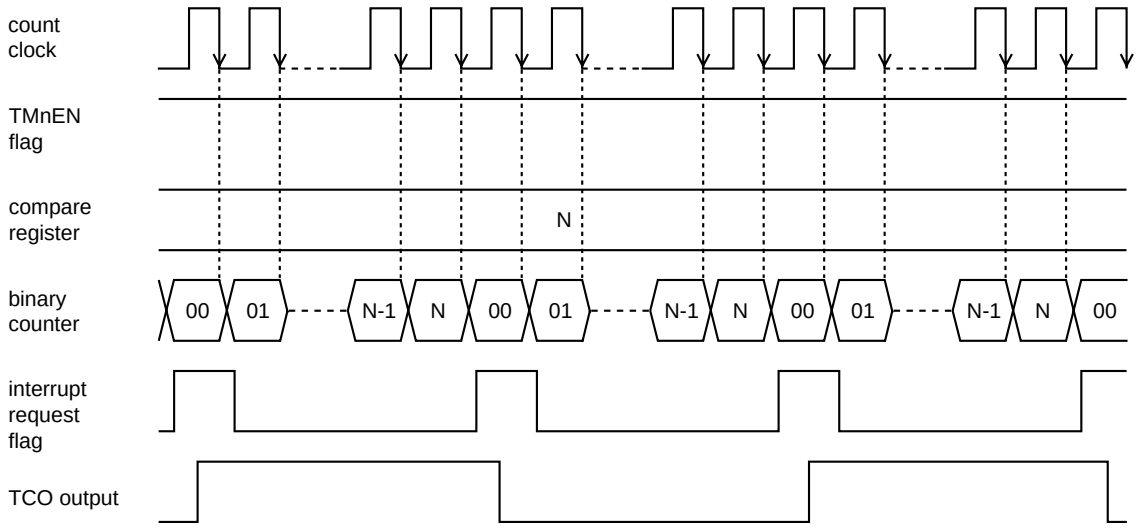


Figure 5-4-1 Count Timing of Timer Pulse Output (Timer 2, Timer 3)

TCO outputs the signal with twice cycles to the set value in the compare register. When the binary counter reaches the value of the compare register, the binary counter is cleared to x'00', then TCO output (timer output) is reversed. Inversion of timer output is changed at the rising edge of the count clock. This is happened to form the waveform inside of the micro controller for precise output cycle.

5-4-2 Setup Example

■Timer Pulse Output Setup Example (Timer 2, Timer 3)
TCO outputs a 50 kHz pulse by timer 2. To output a 50 kHz, select fosc as a clock source, and set the 1/2 cycle (100 kHz) to the timer 2 compare register. Operation is at fosc = 4 MHz.
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM2MD (x'04C') bp3 :TM2EN = 0	(1) Set the TM2EN flag of the timer 2 mode register (TM2MD) to "0" to stop timer 2 counting.
(2) Set the special function pin to output. TCOCNT (x'06A') bp1 : TC23OS = 0 bp2 : TCOS = 1 bp3 : RMOS = 0 bp7 : TCOE = 1 P23DIR (x'012') bp6 : P3DIR2 = 1	(2) Set the TCOE flag of the timer 2 output control register (TCOCNT) to "1" to set P32 pin as a special function pin. Set the timer 2 as output source by the TC23OS flag, the RMOS flag and the TCOS flag. Set the P3DIR2 flag of the port 2, port 3 direction control register (P23DIR) to "1" to set output mode If it needs, pull up resister should be added. [☞ Chapter 3. Ports]
(3) Select the normal timer operation. TM2MD (x'04C') bp4 :TM2PWM = 0	(3) Set the TM2PWM flag of the TM2MD register to "0" to select the normal timer operation.
(4) Select the count clock source. TM2MD (x'04C') bp2-0 :TM2CK2-0 = 100	(4) Select fosc as clock source by the TM2CK2-0 flag of the TM2MD register.
(5) Set the timer pulse output cycle. TM2OC (x'054') = x'27'	(5) Set the 1/2 of the timer pulse output cycle to the timer 2 compare register (TM2OC). The value is set to be "40 - 1 = 39 (x'27')" to be 100 kHz by dividing 4 MHz. At that time, the timer 2 binary counter (TM2BC) is cleared to x'00'.
(6) Start the timer. TM2MD (x'04C') bp3 : TM2EN = 1	(6) Set the TM2EN flag of the TM2MD register to "1" to start timer 2.

TM2BC counts up from 'x00'. When TM2BC reaches the setting value of theTM2OC register and is cleared to x'00', TCO output signal is reversed, then TM2BC count up is restarted from x'00'.

The timer pulse output (at TMnOC = x'00') has the same waveform at TMnOC = x'01'.

If any data is written to the compare register during the binary counter is stopped, timer output is reset to "H".

5-5 8-Bit PWM Output

TCO or port 1 outputs the PWM waveform with generating the PWM basic component that is decided by the timing that the binary counter reaches the set value of the compare register and the overflow timing of the binary counter.

5-5-1 Operation

■Operation of 8-Bit PWM Output (Timer 2)

The PWM waveform with an arbitrary duty cycle is generated by setting the duty cycle of PWM "H" period to the timer 2 compare register (TM2OC). The cycle is the period from the full count to the overflow of the 8-bit timer. Table 5-5-1 shows PWM output pins.

Table 5-5-1 Timer Pulse Output Pins

	timer 2
PWM output pin	TCO output pin (P32) P10-P13 pins

■Count Timing of PWM Output (at normal, Timer 2)

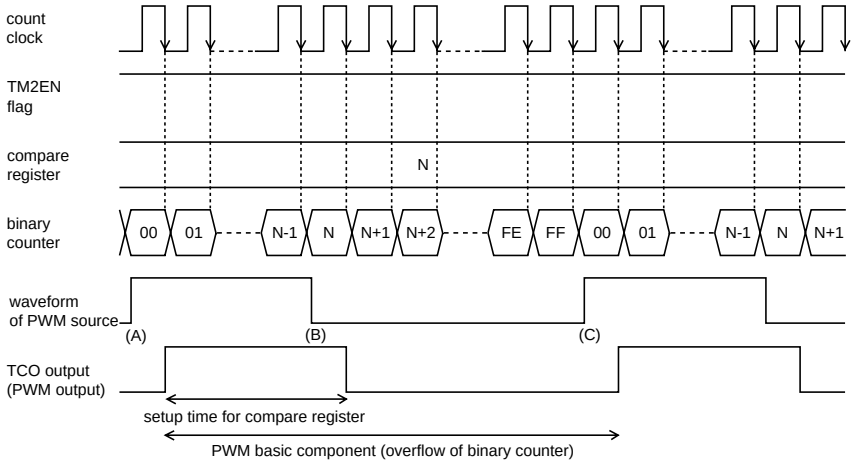


Figure 5-5-1 Count Timing of PWM Output (at normal)

PWM source waveform,

(A) is "H" while counting up from x'00' to the value stored in the compare register.

(B) is "L" after the match to the value in the compare register, then the binary counter continues counting up till the overflow.

(C) is "H" again, if the binary counter is overflown.

The PWM output from pin outputs the PWM source waveform with 1 count clock delay. This is happened, because the waveform is created inside to correct the output cycle.

■Count Timing of PWM Output (when the compare register is x'00') (Timer 2)
Here is the count timing when the compare register is set to x'00' ;

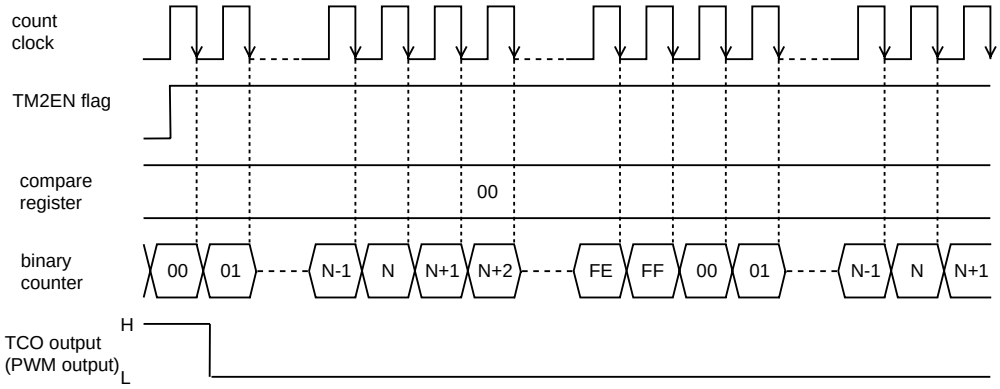


Figure 5-5-2 Count Timing of PWM Output (when compare register is x'00')

When TM2EN flag is stopped ("0") PWM output is "H".

■Count Timing of PWM Output (when the compare register is x'FF') (Timer 2)
Here is the count timing when the compare register is set to x'FF' ;

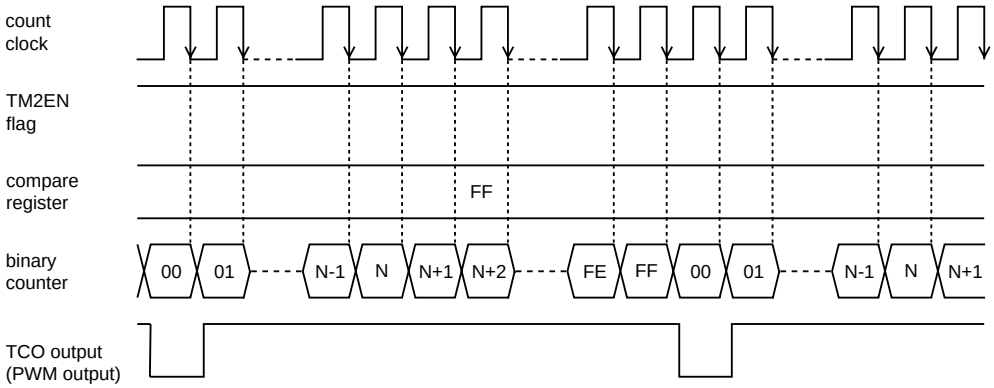


Figure 5-5-3 Count Timing of PWM Output (when compare register is x'FF')

5-5-2 Setup Example

■PWM Output Setup Example (Timer 2)

The 1/4 duty cycle PWM output waveform is output from the TCO output pin at 244 Hz by using timer 2. The oscillation is at low frequency oscillation (fx), at fosc = 4 MHz. Cycle period of PWM output waveform is decided by the overflow of the binary counter. "H" period of the PWM output waveform is decided by the setting value of the compare register.

An example setup procedure, with a description of each step is shown below.

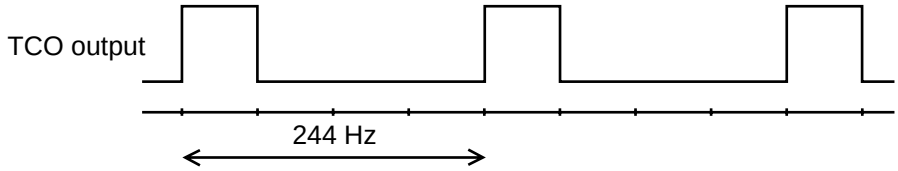


Figure 5-5-4 Output Waveform of TCO Output Pin

Setup Procedure	Description
(1) Stop the counter. TM2MD (x'04C') bp3 :TM2EN = 0	(1) Set the TM2EN flag of the timer 2 mode register (TM2MD) to "0" to stop the timer 2 counting.
(2) Set the special function pin to the output mode. TCOCNT (x'06A') bp1 : TC23OS = 0 bp2 : TCOS = 1 bp3 : RMOS = 0 bp7 : TCOE = 1 P23DIR (x'012') bp6 : P3DIR2 = 1	(2) Set the TCOE flag of the timer output control register (TCOCNT) to "1" to set P32 pin to the special function pin. Set the timer 2 as output source by the TC23OS flag, the TCOS flag and the RMOS flag. Set the P3DIR2 flag of the port 2, port 3 direction control register (P23DIR) to "1" to set output mode [☞ Chapter 3. Ports] If it necessary, add pull-up resistor.
(3) Select the PWM operation. TM2MD (x'04C') bp4 :TM2PWM = 1	(3) Set the TM2PWM flag of the TM2MD register to "1" to select the PWM operation.
(4) Select the count clock source. TM2MD (x'04C') bp2-0 :TM2CK2-0 = 111	(4) Select tosc/64 as clock source by the TM2CK2-0 flag of the TM2MD register.

Setup Procedure	Description
(5) Set the period of PWM "H" output. TM2OC (x'054') = x'40'	(5) Set the "H" period of PWM output to the timer 2 compare register (TM2OC). The setting value is set to 256 / 4 = 64 (x'40'), because it should be the 1/4 duty of the full count (256). At that time, the timer 2 binary counter (TM2BC) is initialized to x'00'.
(6) Start the timer operation. TM2MD (x'04C') bp3 :TM2EN = 1	(6) Set the TM2EN flag of the TM2MD register to "1" to operate timer 2.

TM2BC counts up from x'00'. PWM source waveform outputs "H" till TM2BC reaches the setting value of the TM2OC register, and outputs "L" after that. Then, TM2BC continues counting up, and PWM source waveform outputs "H" again, once overflow is happened, and TM2BC restarts counting up from x'00'. TCO outputs the PWM source waveform with 1 count clock delay.

The initial setting of PWM output is changed from "L" output to "H" output at the selection of PWM operation by the TM2PWM flag of the TM2MD register.

5-6 8-Bit Timer Cascade Connection

5-6-1 Operation

Cascading timers 2 and 3 forms a 16-bit timer.

■8-Bit Timer Cascade Connection Operation (Timer 2 + Timer 3)
Timer 2 and timer 3 are combining to be a 16-bit timer. Cascading timer is operated at clock source of timer 2 which are lower 8 bits.

Table 5-6-1 Timer Functions at Cascade Connection

	timer 2 + timer 3 (16-bit)
interrupt factor	interrupt 3 (IRQ3)
timer operation	√
timer pulse output	√ (TCO output, P10-P13)
high precision PWM output	√
clcok source	fsys/2 fsys/8 fsys/32 fsys/128 fosc fosc/4 fosc/16 fosc/64
fosc : machine clock (oscillation for operation) fsys : system clock	

At cascade connection, the binary counter and the compare register are operated as a 16 bit register. At operation, set the TMnEN flag of the mode register for both of the upper 8-bit timer (timer 3) and lower 8-bit timer (timer 2) to "1" to be operated.
Also, select the clock source by the lower 8-bit timer.
Other setup and count timing is the same to the 8-bit timer at independently operation.

When timer 2 and timer 3 are used in cascade connection, an interrupt request flag is used with timer 3. Timer pulse output of timer 2 is "H" fixed output.

5-6-2 Setup Example

■Cascade Connection Timer Setup Example (Timer 2 + Timer 3)

Setting example of timer function that an interrupt is constantly generated by cascade connection of timer 2 and timer 3, as a 16-bit timer is shown below. An interrupt is generated every 1/2500 cycles by selecting fsys/8 as source clock.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM2MD (x'04C') bp3 : TM2EN = 0 TM3MD (x'04E') bp3 : TM3EN = 0	(1) Set the TM2EN flag of the timer 2 mode register (TM2MD) to "0", the TM3EN flag of the timer 3 mode register to "0" to stop timer 2 and timer 3 counting.
(2) Select the normal lower timer operation. TM2MD (x'04C') bp4 : TM2PWM = 0	(2) Set the TM2PWM flag of the TM2MD register to "0" to select the normal timer 2 operation.
(3) Set the cascade connection. TM3MD (x'04E') bp4 :TM3CAS = 1	(3) Set the TM3CAS flag of the TM3MD register to "1" to connect timer 2 and timer 3 in cascade connection.
(4) Select the count clock source. TM2MD (x'04C') bp2-0 :TM2CK2-0 = 001	(4) Set fsys/8 as clock source by the TM2CK2-0 flag of the TM2MD register.
(5) Set the interrupt generation cycle TM3OC (x'056') =x'09' TM2OC (x'054') =x'C3'	(5) Set the interrupt generation cycle (x'09C3' : 2500 cycles - 1) to the timer 3 compare register + timer 2 compare register (TM3OC + TM2OC). At that time, timer 3 binary counter + timer 2 binary counter (TM3BC + TM2BC) are initialized to x'0000'.
(6) Set the interrupt source. IRQC1 (x'036') bp1-0 : IRQ3S1-0 = 10	(6) Set the IRQ3S1-0 flag of the interrupt control register 1 (IRQC1) to "10" to set timer 3 as an interrupt source.
(7) Clear the interrupt request flag. IRQM (x'032') bp7 : IFIRQ3E = 1	(7) Set the IFIRQ3E flag of the IRQ mode register (IRQM) to "1" to clear the interrupt 3 request flag.

Setup Procedure	Description
(8) Enable the interrupt.	(8) Execute EDI instruction to enable interrupt 3 (IRQ3).
(9) Start the upper timer operation. TM3MD (x'04E') bp3 :TM3EN = 1	(9) Set the TM3EN flag of the TM3MD register to "1" to start timer 3.
(10) Start the lower timer operation. TM2MD (x'04C') bp3 :TM2EN = 1	(10) Set the TM2EN flag of the TM2MD register to "1" to start timer 2.

TM3BC + TM2BC counts up from x'0000' as a 16-bit timer. When TM3BC + TM2BC reaches the set value of TM3OC + TM2OC register, the interrupt 3 request flag is set at the next count clock, and the value of TM3BC + TM2BC becomes x'0000' and restarts count up.

When any data is set to the compare register, set data to both of TM3OC and TM2OC.

Start the upper timer operation before the lower timer operation.

5-7 Remote Control Carrier Output

5-7-1 Operation

Carrier pulse for remote control can be generated.

■Operation of Remote Control Carrier Output (Timer 2, Timer 3)
Remote control carrier pulse is generated with output signal of timer 2 or timer 3. Duty cycle is selected from 1/2, 1/3. At output to port, select the base timer output by the timer output control register (TCOCNT x'06A), and set the remote control output by the RMOS flag.

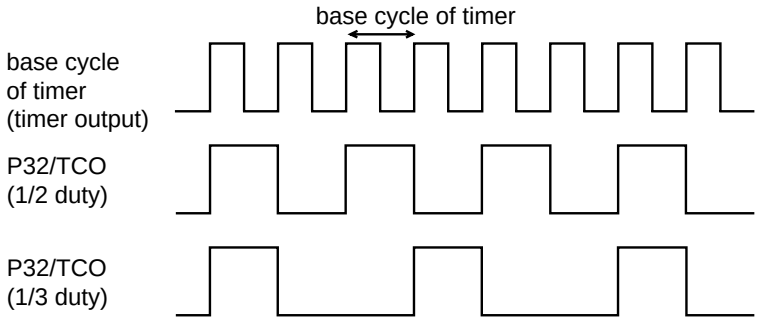


Figure 5-7-1 Duty cycle of Remote Control Carrier Output Signal

■Count Timing of Remote Control Carrier Output (Timer 2, Timer 3)

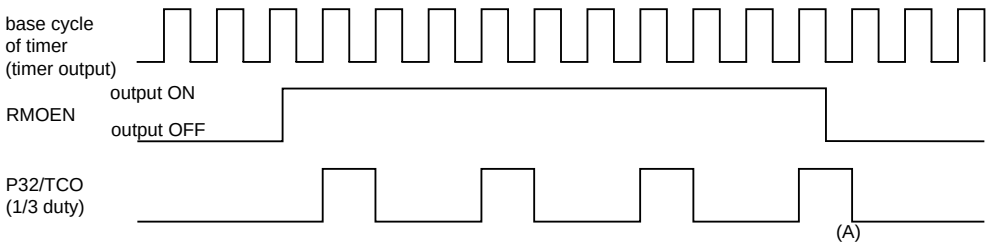


Figure 5-7-2 Count Timing of Remote Control Carrier Output Function (Timer 2, Timer 3)

(A) Even if the RMOEN flag is off when the carrier output is high, the carrier waveform is held by the synchronous circuit.

When the RMOEN flag is changed, do not change the base cycle and its duty at the same time. If they are changed at the same time, the carrier waveform is not output properly.

Buzzer output cannot be set as the base cycle of remote control.

5-7-2 Setup Example

■Remote Control Carrier Output Setup Example (Timer 2, Timer 3)
Here is the setting example that the TCO pin outputs the 1/3 duty carrier pulse signal with "H" period of 36.7 kHz, by using timer 2. The source clock of timer 2 is set as fosc=8 MHz.
An example setup procedure, with a description of each step is shown below.

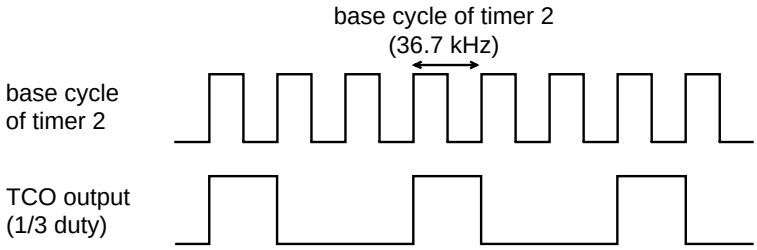


Figure 5-7-3 Output Wave Form of TCO Output Pin

Setup Procedure	Description
(1) Disable the remote control carrier output. TCOCNT (x'06A') bp6 : RMOEN = 0	(1) Set the RMOEN flag of the timer output control register (TCOCNT) to "0" to disable the remote control carrier output.
(2) Stop the counter. TM2MD (x'04C') bp3 : TM2EN = 0	(2) Set the TM2EN flag of the timer 2 mode register (TM2MD) to "0" to stop the timer 2 counting.
(3) Select the base cycle setting timer. TCOCNT (x'06A') bp1 : TC23OS = 0 bp2 : TCOS = 1	(3) Set the timer 2 as a base cycle setting timer by the TC23OS flag and TCOS flag of the TCOCNT register.
(4) Select the carrier output duty. TCOCNT (x'06A') bp5 : RMDTY = 1	(4) Set the RMDTY flag of the TCOCNT register to "1" to select 1/3 duty.
(5) Set the output pin. P23DIR (x'012') bp6 : P3DIR2 = 1 TCOCNT (x'06A') bp3 : RMOS = 1 bp7 : TCOE = 1	(5) Set the P3DIR2 flag of the port 2, port 3 direction control register (P23DIR) to "1" to set P32 for output mode. Set the RMOS flag and TCOE flag of the TCOCNT register to "1".

Setup Procedure	Description
(6) Select the normal timer operation. TM2MD (x'04C') bp4 : TM2PWM = 0	(6) Set the TM2PWM flag of the TM2MD register to "0" to select the normal timer operation.
(7) Select the count clock source. TM2MD (x'04C') bp2-0 : TM2CK2-0 = 100	(7) Select fosc as clock source by the TM2CK2-0 flag of the TM2MD register.
(8) Set the base cycle of remote control carrier. TM2OC (x'054') = x'6C'	(8) Set the base cycle of remote control carrier by writing x'6C' to the timer 2 compare register (TM2OC). The set value should be (8 MHz/ 73.4 kHz) - 1 = 108(x'6C'). So, 8 MHz is divided to be 73.4 kHz, 2 times 36.7 kHz.
(9) Enable the remote control carrier output. TCOCNT (x'06A') bp6 : RMOEN = 1	(9) Set the RMOEN flag of the TCOCNT register to "1" to enable the remote control carrier output.
(10) Start the timer operation. TM2MD (x'04C') bp3 : TM2EN = 1	(10) Set the TM2EN flag of the TM2MD register to "1" to stop the timer 2 counting.

TM2BC counts up from x'00'. Timer 2 outputs the base cycle pulse set in TM2OC. Then, the 1/3 duty remote control carrier pulse signal is output.

5-8 High Precision PWM Output

5-8-1 Operation

PWM waveform is generated by setting the PWM duty to the timer 2 compare register (TM2OC) and setting the PWM cycle to the timer 3 compare register (TM3OC).
Port outputs "H" till the value of the 8-bit binary counter reaches the set value in the timer 2 compare register, then outputs "L" till the value reaches the set value in the timer 3 compare register and the counter is cleared.

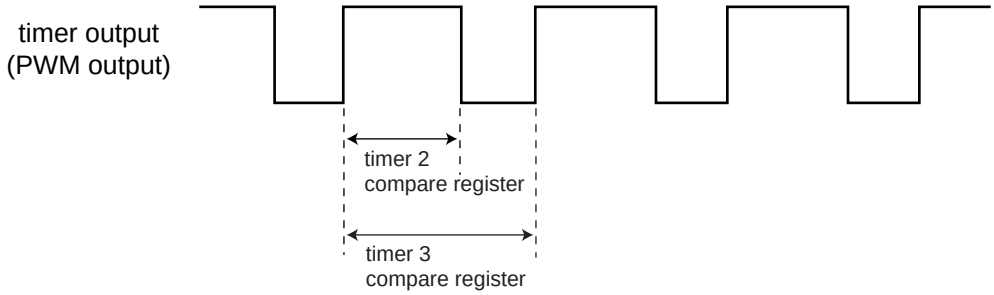


Figure 5-8-1 Count Timing of High Precision PWM Output

The set value in the timer 3 compare register (TM3OC) should be bigger than the one in the timer 2 compare register (TM2OC).

5-8-2 Setup Example

■High Precision PWM Output Setup Example (Timer 2 + Timer 3)
High precision PWM output waveform is output to P10 / PWMO0 pin by cascading timer 2 and timer 3. Then, "fosc" is selected as clock source, and each data is set to both of the timer 2 compare register (TM2OC) and the timer 3 compare register (TM3OC).
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM2MD (x'04C') bp3 : TM2EN = 0 TM3MD (x'04E') bp3 : TM3EN = 0	(1) Set the TM2EN flag of the timer 2 mode register (TM2MD) and the TM3EN flag of the timer 3 mode register (TM3MD) to "0" to disable the timer 2 and timer 3 counting.
(2) Select the lower timer PWM operation. TM2MD (x'04C') bp4 : TM2PWM = 1	(2) Set the TM2PWM flag of the TM2MD register to "1" to select the PWM operation.
(3) Set the cascade connection. TM3MD (x'04E') bp4 : TM3CAS = 1	(3) Set the TM3CAS flag of the TM3MD register to "1" to connect timer 2 and timer 3 in cascade connection.
(4) Set the output pin. P01DIR (x'010') bp6 : P1DIR0 = 1 PORT01 (x'000') bp4 : P10DATA = 1 BZCTR (x'06C') bp0 : PWME10 = 1 MODCNT (x'05E') bp2 : PWMOS0 = 0	(4) Set the P1DIR0 flag of the port 0, port 1 direction control register (P01DIR) to "1" to set P10 for output mode. Set the P10DATA flag of the port 0, port 1 data register (PORT01) to "1" to output "H". Enable the PWM output to port 10 by the PWME10 flag of the BZCTR register and select the timer 2 output by the PWMOS0 flag of the MODCNT register.
(5) Select the count clock source. TM2MD (x'04C') bp2-0 : TM2CK2-0 = 100	(5) Set fosc as clock source by the TM2CK2-0 flag of the TM2MD register.
(6) Set the PWM duty. TM2OC (x'054') = x'55'	(6) Set x'55' to the timer 2 compare register (TM2OC) to set the PWM duty.

Setup Procedure	Description
(7) Set the PWM cycle. TM3OC (x'056') = x'AA'	(7) Set x'AA' to the timer 3 compare register (TM3OC) to set the PWM cycle.
(8) Start the timer 3 operation. TM3MD (x'04E') bp3 : TM3EN = 1	(8) Set the TM3EN flag of the TM3MD register to "1" to start the timer 3.
(9) Start the timer 2 operation. TM2MD (x'04C') bp3 : TM2EN = 1	(9) Set the TM2EN flag of the TM2MD register to "1" to start the timer 2.

5-9 Buzzer Output

5-9-1 Operation

Clock that the source oscillation (fosc) is divided by 1024 / 2048 / 4096, can be output to pin.

■Buzzer Output Operation

Buzzer output frequency is selected by the BZCK1-0 flag of the buzzer output control register (BZCTR), and set the TCOE flag , the RMOS flag and the TCOS flag of the timer output control register (TCOCNT). Set P32 to output mode. The pulse with frequency that selected by the buzzer output pin P32 / BZ is output.

The initial value of buzzer output, the duration till the first rising and falling are indefinite.

5-9-2 Setup Example

■Buzzer Output Setup Example

The buzzer output pin P32 / TCO / BZ outputs clock that the source oscillation fosc is divided by 2048. An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the buzzer output. TCOCNT (x'06A') bp7 : TCOE = 0	(1) Set the TCOEN flag of the timer output control register (TCOCNT) to "0" to stop the buzzer output.
(2) Set the pin. P23DIR (x'012') bp6 : P3DIR2 = 1	(2) Set the P3DIR2 flag of the port 2, port 3 direction control register (P23DIR) to "1" to set P32 to output mode.
(3) Select the buzzer output frequency. BZCTR (x'06C') bp5-4 : BZCK1-0 = 10	(3) Select fosc/2048 as buzzer output frequency by the BZCK1-0 flag of the BZCTR register.
(4) Start the buzzer output operation. TCOCNT (x'06A') bp2 : TCOS = 0 bp3 : RMOS = 0 bp7 : BZOE = 1	(4) Set the TCOE flag, the RMOS flag and the TCOS flag of the timer output control register (TCOCNT) to start buzzer output.

Chapter 6 A/D Converter

6

6-1 Overview

This LSI has an A/D converter with 10 bits resolution. That has a built-in sample hold circuit, and software can switch channel 0 to 3 (AN0 to AN3) to analog input. As A/D converter is stopped, the power consumption can be reduced by a built-in ladder resistance.

6-1-1 Functions

Table 6-1-1 shows the A/D converter functions.

Table 6-1-1 A/D Converter Functions

A/D input pins	4 pins
Pins	AD3 to AD0
Resolution	10 bits
Conversion time (min.)	12.0 μs (at fosc=4 MHz divided by 4)
Input range	V_{SS} to V_{DD}
Save power comsumption	Built-in Ladder Resistance (ON/OFF)

6-1-2 Block Diagram

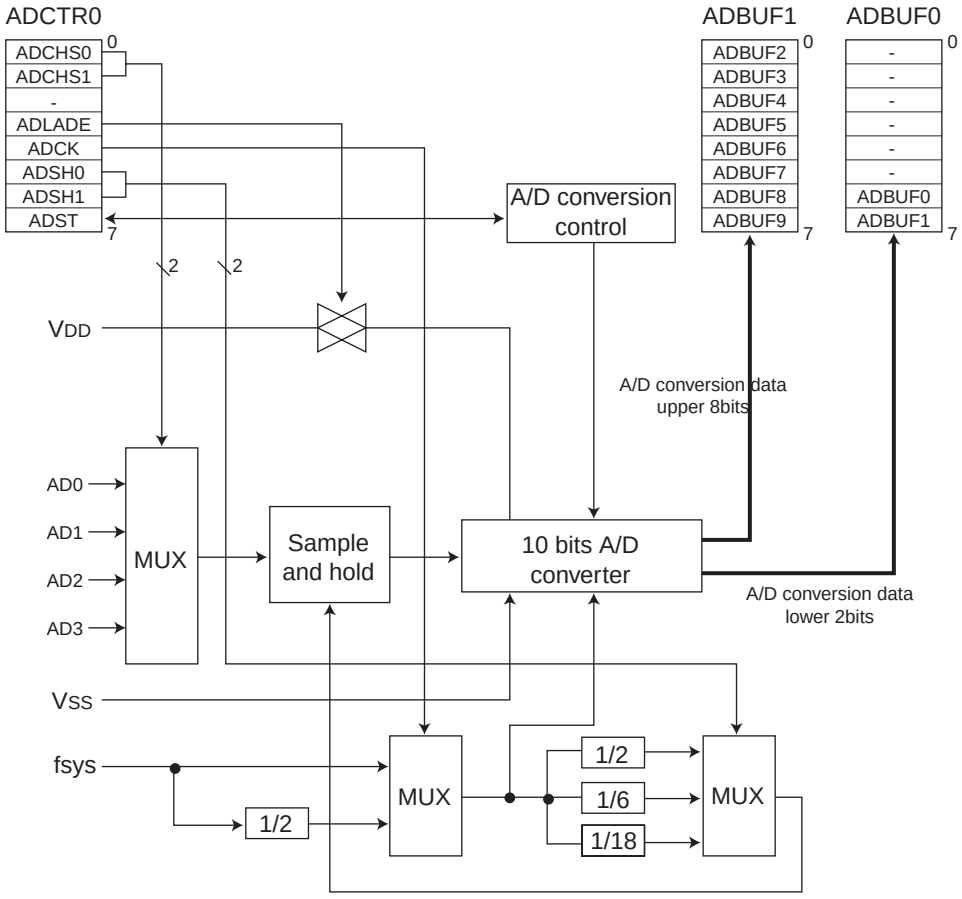


Figure 6-1-1 A/D Converter Block Diagram

6-2 Control Registers

6-2-1 Registers

Table 6-2-1 A/D Converter Control Registers

Register	Address	R/W	Function	Page
ADBUF0	x'070'	R	A/D conversion data storage buffer 0	VI - 6
ADBUF1	x'072'	R	A/D conversion data storage buffer 1	VI - 6
ADCTR0	x'074'	R/W	A/D control register	VI - 5
P23DIR	x'012'	R/W	Port 2, port 3 direction control register	III - 13

6-2-2 Control Registers

■A/D Converter Control Register (ADCTR0)

	7	6	5	4	3	2	1	0
ADCTR0	ADST	ADSH1	ADSH0	ADCK	ADLADE	-	ADCHS1	ADCHS0

(at reset : XXXX0XXX)

ADCHS1	ADCSH0	A/D conversion input selection
0	0	AD0
	1	AD1
1	0	AD2
	1	AD3

ADLADE	A/D ladder resistance connection
0	no connected
1	connected

ADCK	A/D conversion clock selection
0	fsys
1	fsys/2

ADSH1	ADSH0	Sample and hold time
0	0	T_{AD} x 2
0	1	T_{AD} x 6
1	0	T_{AD} x 18
1	1	Reserved

ADST	A/D conversion status
0	stop
1	start

Figure 6-2-1 A/D Control Register (ADCTR0 : x'074', R/W)

6-2-3 Data Buffers

■A/D Conversion Data Storage Buffer 0 (ADBUF0)

The lower 2 bits from the result of A/D conversion are stored to this register.

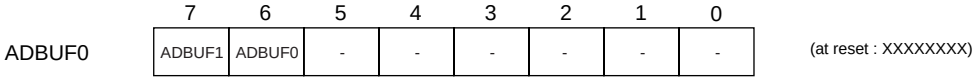


Figure 6-2-2 A/D Conversion Data Storage Buffer 0 (ADBUF0 : x'070', R)

■A/D Conversion Data Storage Buffer 1 (ADBUF1)

The upper 8 bits from the result of A/D conversion are stored to this register.

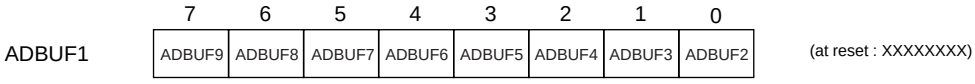


Figure 6-2-3 A/D Conversion Data Buffer 1 (ADBUF1 : x'072', R)

6-3 Operation

Here is a description of A/D converter circuit setup procedure.

(1) Set the analog pins.
Set the analog input pin to input mode by the port 2, port 3 direction control register (P23DIR) and set the port 2, port 3 output structure register (P23PLU) to "0" to select pull-up resistor "OFF".
Setup for the port 2, port 3 direction control register (P23DIR) should be done before analog voltage is put to pins.

(2) Set the A/D conversion input pin.
Select the analog input pin from AD3 to AD0 by the ADCHS1 to ADCHS0 flag of the A/D converter control register (ADCTR0).

(3) Select the A/D converter clock.
Select the A/D converter clock by the ADCK flag of the A/D converter control register (ADCTR0).
Depending on the resonator, the converter clock (TAD) should not be under 800 ns.

(4) Set the sample hold time.
Set the sample hold time by the ADSH1, ADSH0 flag of the A/D converter control register (ADCTR0). The sample hold time should be based on analog input impedance.

(5) Set the A/D ladder resistance.
Set the ADLADE flag of the A/D converter control register (ADCTR0) to "1", and through current to the ladder resistance for A/D conversion.

(2) to (5) are not in order, can be operated simultaneously.

(6) Start the A/D conversion.
Set the ADST flag of the A/D control register (ADCTR0) to "1" to start the A/D conversion.

(7) A/D conversion
After sampling with the sample and hold time, set in (4), A/D conversion is decided in comparison with MSB, in order.

(8) Complete the A/D conversion.
When A/D conversion is finished, the ADST flag is cleared to "0", and the result of the conversion is stored to the A/D buffer (ADBUF0, 1).

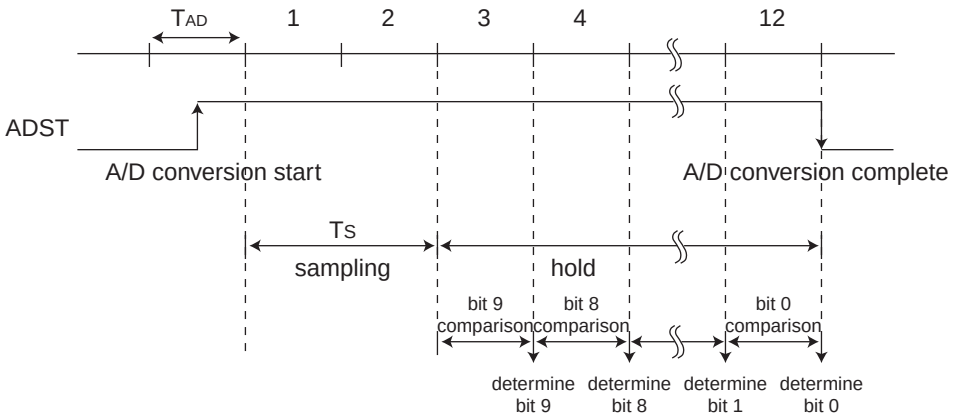


Figure 6-3-1 Timing of A/D Conversion (Ts = TAD x 2)

To read out the value of the A/D conversion, A/D conversion should be done several times to prevent noise by confirming the match of the level by program, or by using the average value.

6-3-1 Setup

■Input Pins of A/D Converter Setup

Input pins for A/D converter is selected by the ADCHS1 to 0 flag of the ADCTR0 register.

Table 6-3-1 Input Pins of A/D Converter Setup

ADCHS1	ADCHS0	A/D pin
0	0	AD0 pin
	1	AD1 pin
1	0	AD2 pin
	1	AD3 pin

■Clock of A/D Converter Setup

The A/D converter clock is set by the ADCK flag of the ADCTR0 register. Set the A/D converter clock (T_{AD}) more than 1 µs . Table 6-3-2 shows the machine clock (fosc) and the A/D converter clock (T_{AD}). (calculated as fsys = fosc/4)

Table 6-3-2 A/D Conversion Clock and A/D Conversion Cycle

ADCK	A/D conversion clock	A/D conversion cycle (T_{AD})	
		at fosc=4 MHz (divided by 4)	at fosc=8 MHz (divided by 4)
0	fsys	1.00 µs	500.00 ns (no usable)
1	fsys/2	2.00 µs	1.00 µs

For the system clock (fsys), refer to Chapter 2. 2-4 Clock Switching.

■Sampling Time (Ts) of A/D Converter Setup

The sampling time of A/D converter is set by the ADSH1 to 0 flag of the ADCTR0 register. The sampling time of A/D converter depends on external circuit, so set the right value by analog input impedance.

Table 6-3-3 Sampling Time of A/D Conversion and A/D Conversion Time

ADSH1	ADSH0	Sampling time (Ts)	A/D conversion time	
			at TAD=1.00 µs	at TAD=2.00 µs
0	0	TAD x 2	12.00 µs	24.00 µs
	1	TAD x 6	16.00 µs	32.00 µs
1	0	TAD x 18	28.00 µs	56.00 µs
	1	Reserved	-	-

■Built-in Ladder Resistance Control

The ADLADE flag of the ADCTR0 register is set to "1" to send a current to the ladder resistance for A/D conversion. As A/D converter is stopped, the ADLADE flag of the ADCTR0 register is set to "0" to save the power consumption.

Table 6-3-4 A/D Ladder Resistance Control

ADLADE	A/D ladder resistance control
0	A/D ladder resistance OFF (A/D conversion stop)
1	A/D ladder resistance ON (A/D converison stand by)

■A/D Conversion Starting Setup

A/D conversion starting is set by the ADST flag of the ADCTR0 register. The ADST flag of the ADCTR0 register is set to "1" to start A/D conversion. The ADST flag of the ADCTR0 register is set to "1" during A/D conversion, then cleared to "0" as the A/D conversion is completed.

Table 6-3-5 A/D Conversion Starting

ADST	A/D conversion activation factor
0	A/D conversion completed or stopped
1	A/D conversion started or in progress

6-3-2 Setup Example

■A/D Converter Setup Example by Registers

A/D conversion is started by setting registers. The analog input pins are set to AD0, the conversion clock is set to fsys/2, and the sample and hold time is set to TAD x 6.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the analog input pin. P23DIR (x'012') bp0 : P2DIR0 = 0	(1) Set P20 / AD0 pin to the input mode by the port 2, port 3 direction control register (P23DIR).
(2) Select the analog input pin. ADCTR0 (x'074') bp1-0 : ADCHS1-0 = 00	(2) Select AD0 to the analog input pin by the ADCHS1-0 flag of the A/D converter control register (ADCTR0).
(3) Select the A/D conversion clock. ADCTR0 (x'074') bp4 : ADCK = 1	(3) Select fsys/2 to the A/D conversion clock by the ADCK flag of the A/D converter control register (ADCTR0).
(4) Set the sample and hold time. ADCTR0 (x'074') bp6-5 : ADSH1-0 = 01	(4) Set TAD x 6 to the sample and hold time by the ADSH1, ADSH0 flag of the A/D converter control register (ADCTR0).
(5) Set the A/D ladder resistance. ADCTR0 (x'074') bp3 : ADLADE = 1	(5) Set the ADLADE flag of the A/D converter control register (ADCTR0) to "1" to send a current to the ladder resistance for the A/D conversion.
(6) Start the A/D conversion. ADCTR0 (x'074') bp7 : ADST = 1	(6) Set the ADST flag of the A/D converter control register (ADCTR0) to "1" to start the A/D conversion.
(7) Complete the A/D conversion. ADBUF0 (x'070') ADBUF1 (x'072')	(7) The ADST flag of the A/D control register (ADCTR0) is cleared to "0" as the A/D conversion is completed. The result is stored to the A/D buffer (ADBUF0, 1).

6-3-3 Cautions

A/D conversion can be damaged by noise easily, hence antinoise transaction should be operated.

■Antinoise transaction
For A/D input (analog input pin), add condenser near the VSS pins of micro controller.

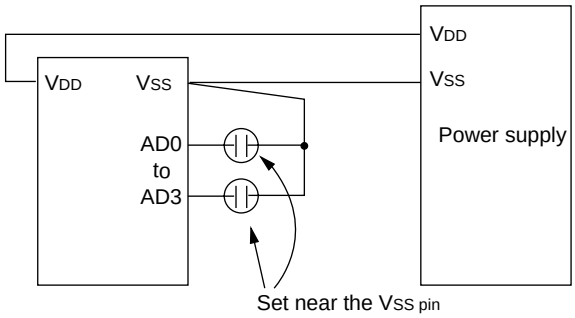
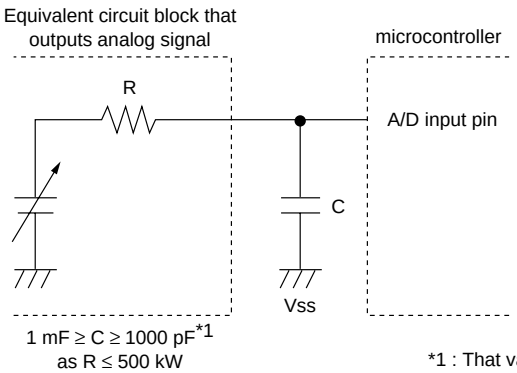


Figure 6-3-2 A/D Converter Recommended Example

For high precision of A/D conversion, the following cautions on A/D converter should be kept.

1. The input impedance R of A/D input pin should be under 500 kΩ *1, and the external capacitor C (more than 1000 pF, under 1μF *1).
2. The A/D conversion frequency should be set with consideration of R, C.
3. At the A/D conversion, if the output level of micro controller is changed, or the peripheral added circuit is switched to ON/OFF, the A/D conversion may work wrongly, because the analog input pins and power pins do not fix. At the check of the setup, confirm the waveform of analog input pins.
4. Start the A/D conversion after A/D ladder resistance is connected and about 1 ms is taken.



A/D Converter Recommended Example

Chapter 7 AC Zero-Cross Detection

7-1 Overview

7-1-1 Overview

This LSI has a set of AC zero-cross detection circuit.
The ACZ pin is the input pin of AC zero-cross detection circuit.
AC zero-cross detection circuit outputs the high level when the input level is at the middle, and outputs the low level at other level.
The ACZ pin is connected to P31 input circuit, too. So It can be read out by program.
The ACZ input circuit is connected to the input clamp diode.

The ACZ interrupt is generated at the rising or falling edge of the AC zero-cross detection output.
When the ACZ interrupt is used, select ACZ as an interrupt source by the interrupt control register 1 (IRQC1), and specify the edge, and enable the interrupt 3 (IRQ3) by the EDI instruction.

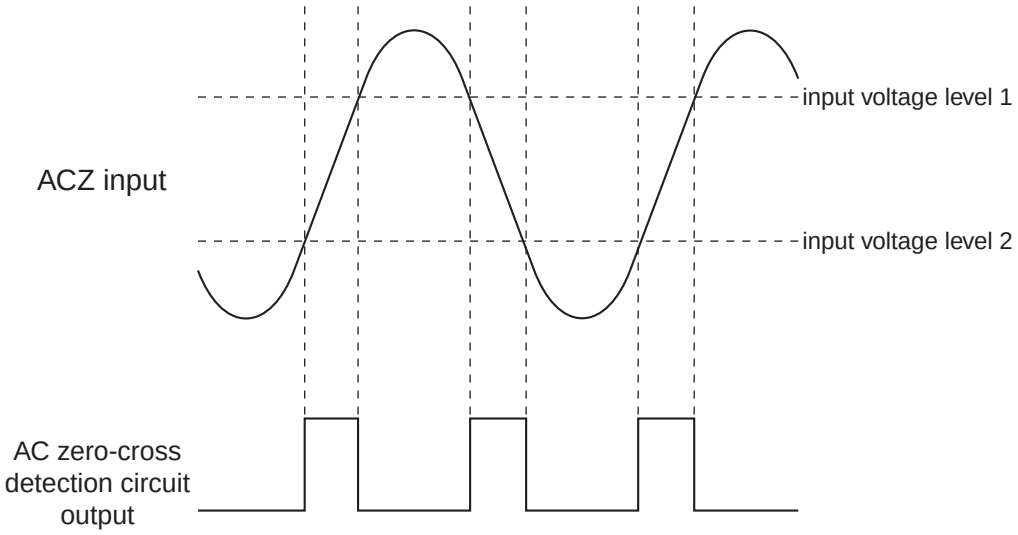


Figure 7-1-1 A/C Zero-Cross Detection Circuit Timing Chart

7-1-2 Block Diagram

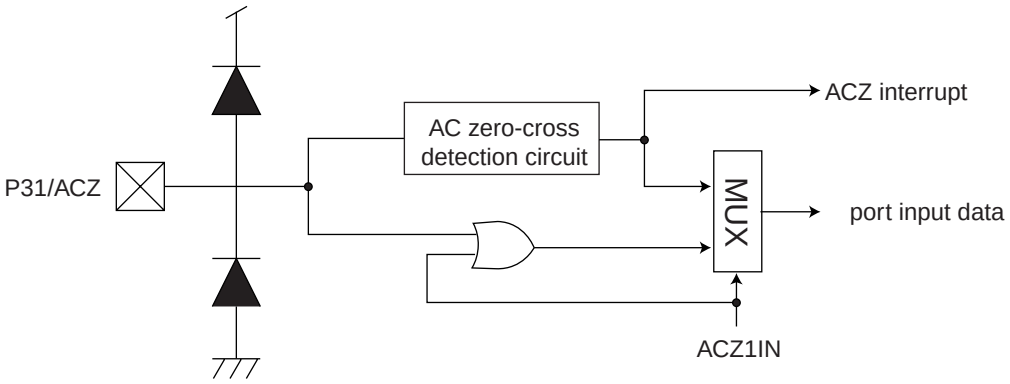


Figure 7-1-2 A/C Zero-Cross Detection Circuit Block Diagram

7-1-3 Operation

Setup procedure and its description are as follows.

■ACZ

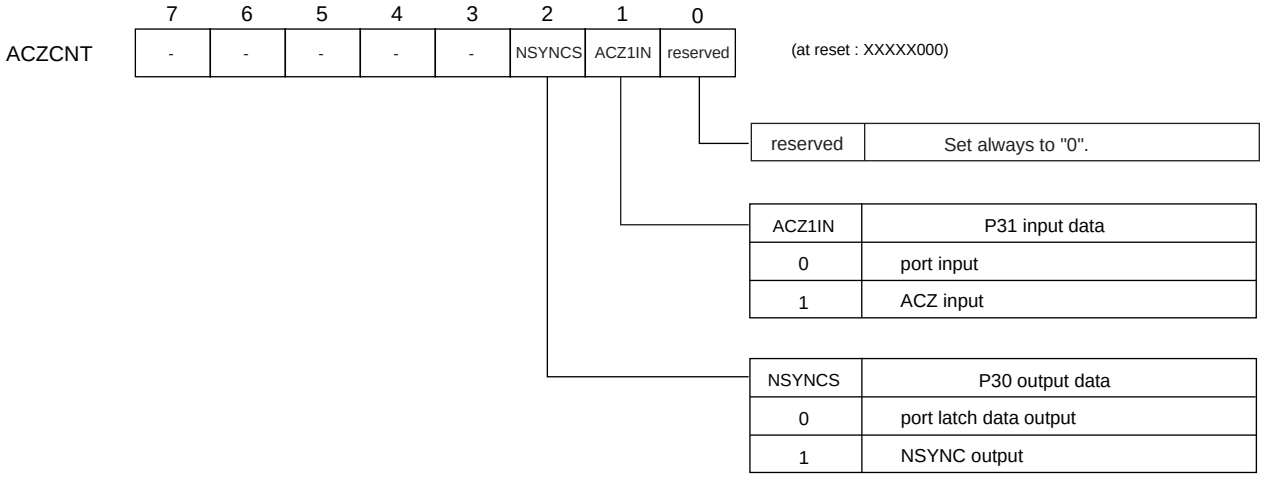
(1) Set the pin's direction.
Set the P3DIR1 flag of the port 3 direction control register (P23DIR) to "0" to set P31 to input mode.

(2) Switch the P31 input data.
Select the ACZ input by the ACZ1IN flag of the ACZ control register (ACZCNT).

(3) Set the ACZ interrupt.
Set the interrupt source by the interrupt control register 1 (IRQC1).
Set the IRQ3S1-0 flag to "01" to select the ACZ input. Select the interrupt edge by the IRQ3SE flag and set the MASKIR3 flag to "1" to enable the interrupt edge mask.
Enable the interrupt 3 (IRQ3) by the EDI instruction.

[☞ Chapter 4. 4-2 Interrupt Control Register]

7-2 Control Registers



ACZ Control Register (ACZCNT : x'03A', R/W)

Table 7-2-1 AC Zero-Cross Detection Control Register

Chapter 8 Watchdog Timer

8-1 Overview

8-1-1 Overview

This LSI has a watchdog timer to detect errors in program.
The watchdog timer always counts, and outputs the low level for reset after 2^{16} counts of machine cycle.
Therefore, the watchdog timer is restarted several times during programing to detect errors.
Restarting is done by writing "1" to the WDTCLR flag of the watchdog timer control register (WDCTR).

The watchdog timer is stopped at HALT mode, STOP mode.

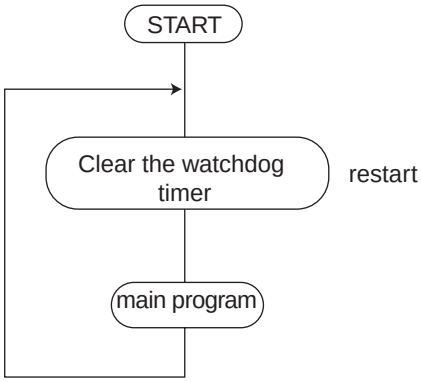


Figure 8-1-1 Flow Chart

8-1-2 Block Diagram

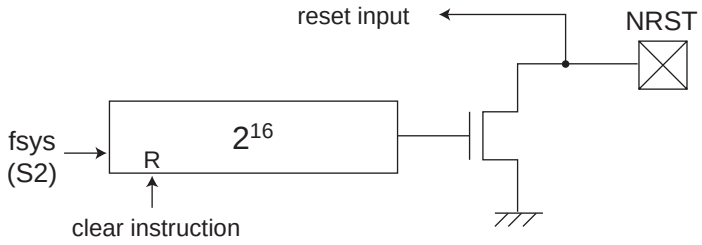
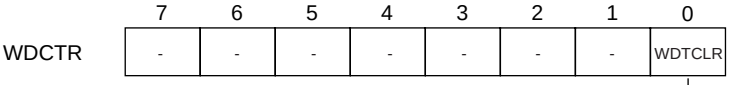


Figure 8-1-2 Watchdog Timer Block Diagram

8-2 Control Registers



WDTCLR	clear the watchdog timer
0	operate
1	clear

Watchdog Timer Control Register (WDCTR : x'06E', W)

Figure 8-2-1 Watchdog Timer Control Register

Chapter 9 Automatic Reset

9-1 Overview

9-1-1 Overview

This LSI has 2 sets of auto-reset circuit that detect low voltage (mask option).
When low voltage (V_{RSTL}) is detected, the NRST pin becomes automatically "L" level for reset.
And if the power supply voltage reaches the reset release voltage (V_{RSTH}), the NRST pin becomes "H" by the hardware, and reset is released.

When the auto-reset circuit 2 is used, the machine cycle should be more than 2 µs.

When the power is supplied, take enough time for the reset pin voltage to be realized as reset signal.

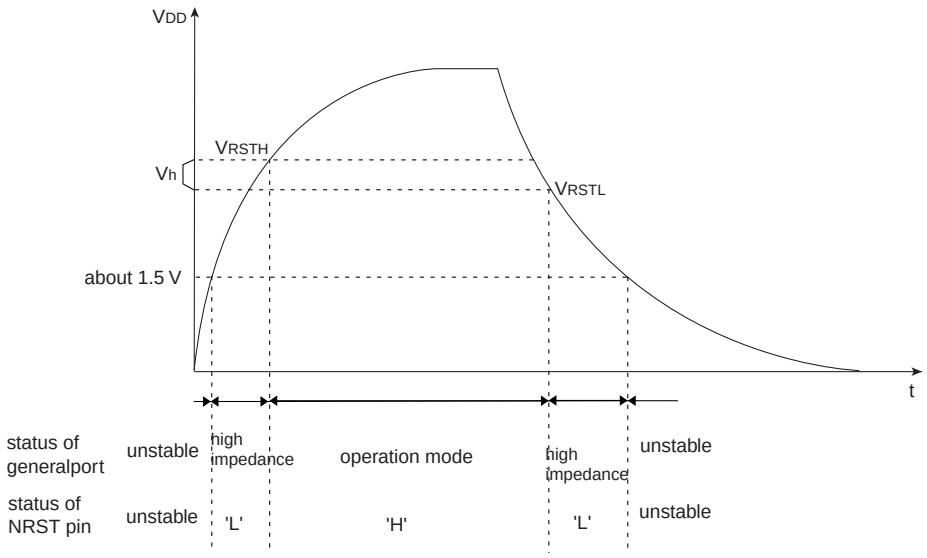


Figure 9-1-1 Automatic Reset Voltage

9-1-2 Electrical Characteristics

Ta = -40 °C to +85 °C V_{DD} = 2.0 V to 5.5 V($V_{RSTL1,2}$ to 5.5 V) V_{SS} = 0 V

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply voltage							
1	Power supply voltage	V_{DD4} *1	fosc ≤ 8 MHz(divided by 4) Automatic reset	V_{RSTL1}	-	5.5	V
2		V_{DD5}	fosc ≤ 4 MHz(divided by 8) Automatic reset	V_{RSTL1} V_{RSTL2}	-	5.5	
*1 Automatic reset 2 can not be selected in mask option.							
Automatic reset circuit 1							
3	Power supply detection level	V_{RSTH1}	figure 9-1-1.	-	3.9	4.40	V
4		V_{RSTL1}		3.20	3.70	-	
5	Hysteresis width	Vh		0.05	0.20	-	
6	Power supply voltage change	Δt / Δ V		1.00	-	-	
Automatic Reset circuit 2							
7	Power supply detection level	V_{RSTH2}	figure 9-1-1.	-	2.20	2.40	V
8		V_{RSTL2}		1.80	2.05	-	
9	Hysteresis width	Vh		0.05	0.15	-	
10	Power supply voltage change	Δt / ΔV		1.00	-	-	ms/V
Power supply current							
11	Automatic reset current consumption *2	I_{DD8}	V_{DD}=5.0 V	-	4	8	μA
*2 I_{DD8} indicates the consumption, normally spent in automatic reset circuit. So if automatic reset is selected, each rating is added.							

Chapter 10 Appendices

10-1 EPROM Version

10-1-1 Overview

EPROM version is microcontroller which was replaced the mask ROM of the MN15G0202, MN15G0402 with an electronically programmable EPROM. These include the MN15G0202, MN15G0402 variants MN15GP0402SJ and PX-AP15G0402-SY.

The MN15GP0402SJ is sealed in plastic. Once data is written to the internal PROM, it cannot be erased. The PX-AP15G0402 is sealed in a ceramic package with a window. Written data can be erased by exposing the physical chip to intense ultraviolet radiation.

Setting the EPROM version to EPROM mode, functions as a microcomputer are halted, and the internal EPROM can be programmed. For EPROM pin connection, refer to figure 19-1-2. Programming Adapter Connection.

The specification for writing to and reading from the internal EPROM are possible by using a dedicated programming adapter (supplied by Panasonic) and Lab Site from Data I/O, after down loading them.

The EPROM Version is described on the following items :

- Cautions on use of the internal EPROM
- Erasing Data in Windowed Package (PX-AP15G0402-SY)
- Differences between mask ROM vers. and EPROM vers.
- Writing to the Microcomputer with internal EPROM
- Cautions on handling a ROM writer

MN15GP0402SJ is available only for engineering sample now. (Mask option is high speed oscillation, no auto reset.)

The PX-AP15G0402-SY with windowed ceramic package is not supplied.

10-1-2 Cautions on Use

EPROM Version differs from the MN15G0202, MN15G0402 in some of its electrical characteristics. The user should be aware of the following cautions :

(1) Due to device characteristics of the MN15GP0402SJ, a writing test cannot be performed on all bits. Therefore, the reliability of data writing may not be 100% ensured.

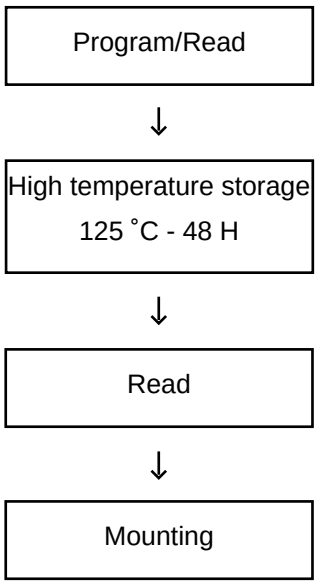
(2) When a program is written, verify that V_{DD} power supply (6 V) is connected before applying the V_{PP} power supply (12.5 V). Disconnect the V_{PP} supply before disconnecting the V_{DD} supply.

(3) V_{PP} should never exceed 13.5 V including overshoot.

(4) If a device is removed while a V_{PP} of +12.5 V is applied, device reliability may be damaged.

(5) At CE=V_{IL}, do not change Vpp from V_{IL} to +12.5 V or from +12.5 V to V_{IL}.

(6) After a program is written, screening at a high temperature storage is recommended before mounting.



10-1-3 Differences between Mask ROM version and EPROM version

The differences between the 4-bit microcontroller MN15G0202, MN15G0402 (Mask ROM vers.) and the microcontroller with internal EPROM are as follows ;

		MN15G0202, MN15G0402 (ROM version)	MN15GP0402 (EPROM version)
Operating ambient temperature		- 40 ˚C to 85 ˚C	- 20 ˚C to 70 ˚C
Operating voltage		3.0 V to 5.5 V (0.50 µs / at 8 MHz, divided by 4) 2.4 V to 5.5 V (1.00 µs / at 8 kHz, divided by 8) 2.0 V to 5.5 V (2.00 µs / at 4 kHz, divided by 8)	3.0 V to 5.5 V (0.50 µs / at 8 MHz, divided by 4) 2.4 V to 5.5 V (1.00 µs / at 8 kHz, divided by 8) 2.3 V to 5.5 V (2.00 µs / at 4 kHz, divided by 8)
Mask option	Auto reset circuit	1. No auto reset 2. Auto reset circuit 1 3. Auto reset circuit 2	1. No auto reset
Pin DC Characteristics		Output current, input current and input judge level are the same.	

There are no other functional differences.

10-1-4 Writing to Microcomputer with Internal EPROM

This LSI needs the dedicated device for writing. The device should be only Data I/O Lab Site, can be used after down loading.

10-1-5 Cautions on Operation of ROM Writer

■Cautions on Handling the ROM writer

(1) The V_{PP} programming voltage for the EPROM versions is 12.5 V.
Programming with a 21 V ROM writer can lead to damage. The ROM writer specifications need the dedicated device for writing.

(2) Make sure that the socket adapter matches the ROM writer socket and that the chip is correctly mounted in the socket adapter. Faulty connections can lead to damage.

(3) After cleaning all memory of the ROM writer, load the program to the ROM writer.
(Data x'FF' is written to the address x'0000' to x'7FFF')

(4) After confirming the device type, write the loaded program in (3) to the address, from microcomputer address x'0000' to the final address of the internal ROM.

The internal ROM space of this LSI is from x'0000'.
[☞ Chapter 2 2-2. Memory Space]

This writer has no internal ID codes of "Silicon Signature" and "Intelligent Identifier" of the auto-device selection command of ROM writer. If the auto-device selection command is to be executed for this writer, the device is likely damaged. Therefore, never use this command.

■When the writing is disabled

When the writing is disabled, check the following points.

(1) Check that the device is mounted correctly on the socket (pin bending, connection failure).

(2) Check that the erase check result is no problem.

(3) Check that the adapter type is identical to the device name.

(4) Check that the dedicated device for writing is used.

(5) Check that the data is correctly transferred to the ROM writer.

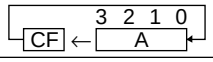
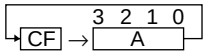
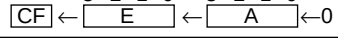
(6) Recheck the check points (1), (2) and (3) provided on the above paragraph of 'Cautions on Handling the ROM writer'.

Please contact the nearest semiconductor design center (See the attached sales office table.), when the writing is disabled even after the above check points are confirmed and the device is replaced with another one.

10-2 Instruction Set

INSTRUCTION	Mnemonic		Operation	Flag		Code Size	Cycle	Machine Code	Page
				CF	ZF				
Data move instructions	L	load	A←M(X,Y)	-	●	1	1	17	43
	LICY	load, increment Y	A←M(X,Y),Y←Y+1	-	●	1	2	21	43
	LDCY	load, decrement Y	A←M(X,Y),Y←Y-1	-	●	1	2	25	44
	LD da	load direct	A←M(da)	-	●	2	2	1F:da	44
	LX	load from X	A←X	-	●	1	1	44	45
	LY	load from Y	A←Y	-	●	1	1	45	45
	LI n	load immediate	A←n (to pile up LI instructions)	-	-	1	1	Fn	46
	LYI n	load Y immediate	Y←n	-	-	1	1	Cn	46
	LEAI mn	load EA immediate	E←m,A←n	-	-	2	2	76:mn	47
	LXYI mn	load XY immediate	X←m,Y←n	-	-	2	2	77:mn	47
	LBD da	load byte direct	E←M(da+1),A←M(da)	-	-	2	2	48:da	48
	ST	store	M(X,Y)←A	-	-	1	1	57	49
	STICY	store, increment Y	M(X,Y)←A,Y←Y+1	-	●	1	2	22	49
	STDCY	store, decrement Y	M(X,Y)←A,Y←Y-1	-	●	1	2	26	50
	STD da	store direct	M(da)←A	-	-	2	2	53:da	50
	STE	store to E	E←A	-	-	1	1	56	51
	STX	store to X	X←A	-	-	1	1	54	51
	STY	store to Y	Y←A	-	-	1	1	55	52
	STBD da	store byte direct	M(da+1)←E,M(da)←A	-	-	2	2	49:da	52
	EX	exchange	A ↔ M(X,Y)	-	-	1	1	47	53
	EXD da	exchange direct	A ↔ M(da)	-	-	2	2	43:da	53
	EXE	exchange E	A ↔ E	-	-	1	1	46	54
	EXSE	exchange SE	E ↔ SE(E ↔ M(0,2))	-	-	1	1	42	54
	EXSX	exchange SX	X ↔ SX(E ↔ M(0,0))	-	-	1	1	40	55
	EXSY	exchange SY	Y ↔ SY(E ↔ M(0,1))	-	-	1	1	41	55
	LBXY z	load byte pointed by XY-register	EA←CR(z,X,Y)	-	-	1	1	4(C+z)	56
	LBDC z, da	load byte direct control register	EA←CR(z,da)	-	-	2	2	2(8+z):da	56
	STBXY z	store byte pointed by XY-register	CR(z,X,Y)←EA	-	-	1	1	5(C+z)	57
	STBDC z, da	store byte direct control register	CR(z,da)←EA	-	-	2	2	2(C+z):da	57
	PSHEA	push E, A	SP←SP-2,M(SP)←EA	-	-	1	1	68	58
	PSHXY	push X, Y	SP←SP-2,M(SP)←XY	-	-	1	1	69	59
	POPEA	pop E, A	EA←M(SP),SP←SP+2	-	-	1	1	6C	60
	POPXY	pop X,Y	XY←M(SP),SP←SP+2	-	-	1	1	6D	61
	LMEI m, n	load and modify E	E←(E&$\overline{m}$)+n	-	●	2	2	33:mn	62
	LMXI m, n	load and modify X	X←(X&$\overline{m}$)+n	-	●	2	2	32:mn	62
	RMD da	reset memory direct	M(da)←0	-	-	2	2	37:da	63
	WTSB	write SB	SB←EA	-	-	1	1	80	✱
	RDSB	read SB	EA←SB	-	-	1	1	84	✱
	WTTB	write TB	TB←EA	-	-	1	1	82	✱
	RDBC	read BC	EA←TB	-	-	1	1	85	✱
	WTSP	write SP	SP←EA	-	-	1	1	05	66
	RDSP	read SP	EA←SP	-	-	1	1	04	66
	RDTBL	read table	EA←ROM(PCh,EA)	-	-	1	2	0B	67
Arithmetic instructions	A	add	A←A+M(X,Y)	●	●	1	1	10	68
	AD da	add direct	A←A+M(da)	●	●	2	2	18:da	68
	AC	add with carry	A←A+M(X,Y)+CF	●	●	1	1	11	69
	ACD da	add direct with carry	A←A+M(da)+CF	●	●	2	2	19:da	69
	AI n	add immediate	A←A+n	●	●	1	1	Dn	70
	S	subtract	A←A-M(X,Y)	●	●	1	1	12	71
	SD da	subtract direct	A←A-M(da)	●	●	2	2	1A:da	71
	SB	subtract with borrow	A←A-M(X,Y)-CF	●	●	1	1	13	72
	SBD da	subtract direct with borrow	A←A-M(da)-CF	●	●	2	2	1B:da	72
	C	compare	A-M(X,Y)...FS	●	●	1	1	0F	73
	CD da	compare direct	A-M(da)...FS	●	●	2	2	0D:da	73
	CEAI mn	compare byte immediate	EA-mn...FS	●	●	2	2	0C:mn	74
	CI n	compare immediate	A-n...FS	●	●	1	1	En	74
	ICM	increment memory	M(X,Y)←M(X,Y)+1	●	●	1	1	60	75
	ICMD da	increment memory direct	M(da)←M(da)+1	●	●	2	2	61:da	75

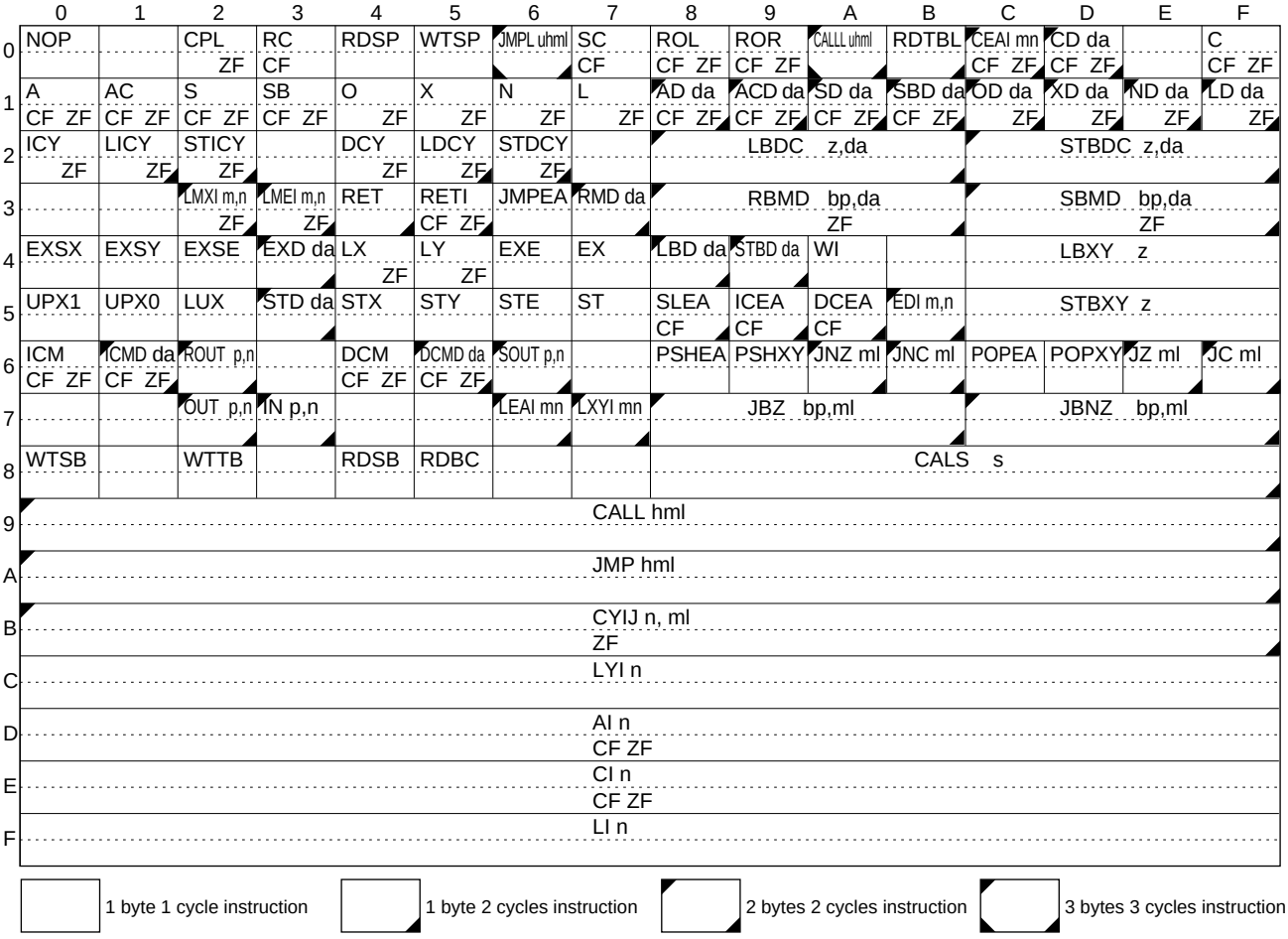
Note : "Page" refers to the corresponding page in the Instruction Manual. But, ✱ marked instruction should be refered to chapter 10-4.

INSTRUCTION	Mnemonic			Operation	Flag		Code Size	Cycle	Machine Code	Page
					CF	ZF				
Arithmetic instructions	ICY		increment Y	Y←Y+1	-	●	1	1	20	76
	ICEA		increment byte	EA←EA+1	●	-	1	2	59	76
	DCM		decrement memory	M(X,Y)←M(X,Y)-1	●	●	1	1	64	77
	DCMD	da	decrement memory direct	M(da)←M(da)-1	●	●	2	2	65:da	77
	DCY		decrement Y	Y←Y-1	-	●	1	1	24	78
	DCEA		decrement byte	EA←EA-1	●	-	1	2	5A	78
	CPL		complement	A←$\overline{A}$	-	●	1	1	02	79
Logical instructions	N		and	A←A & M(X,Y)	-	●	1	1	16	80
	ND	da	and direct	A←A & M(da)	-	●	2	2	1E:da	80
	O		or	A←A | M(X,Y)	-	●	1	1	14	81
	OD	da	or direct	A←A | M(da)	-	●	2	2	1C:da	81
	X		exclusive or	AA & M(X,Y)	-	●	1	1	15	82
	XD	da	exclusive or direct	AA & M(da)	-	●	2	2	1D:da	82
	ROL		rotate left		●	●	1	1	08	83
	ROR		rotate right		●	●	1	1	09	83
	SLEA		shift left byte		●	-	1	2	58	84
Bit manipulation instructions	RBMD	bp, da	reset bit memory direct	M(da)bp←0	-	●	2	2	3(8+bp):da	85
	SBMD	bp, da	set bit memory direct	M(da)bp←1	-	0	2	2	3(C+bp):da	85
Branch instructions	JMP	hml	jump	PCh←h, PCm←m, PCl←l	-	-	2	2	Ah:ml	86
	JMPL	uhml	jump long	PCu←u, PCh←h, PCm←m, PCl←l	-	-	3	3	06:uh:ml	88
	JMPEA		jump by EA	PCm←E, PCl←A	-	-	1	1	36	89
	CALL	hml	call	SP←SP-4, M(SP)←PC+2/CF/ZF/LIFF, PChh, PCmm, PCll	-	-	2	2	9h:ml	91
	CALLL	uhml	call long	SPSP-4, M(SP)PC+2/CF/ZF/LIFF, PCuu, PChh, PCmm, PCll	-	-	3	3	0A:uh:ml	93
	CALS	s	call short	SPSP-4, M(SP)PC+2/CF/ZF/LIFF, PCh←0, PCm←8+s, PCl←0	-	-	1	2	8(8+s)	95
	RET		return	PC←M(SP), SP←SP+4	-	-	1	2	34	
	RETI		return from interrupt	PC/CF/ZF/LIFF←M(SP), SP←SP+4	●	●	1	2	35	
	JZ	ml	jump if zero	if ZF=1, PCm←m, PCl←l if ZF=0, PC←PC+2	-	-	2	2	6E:ml	100
	JNZ	ml	jump if nonzero	if ZF=0, PCmm, PCll if ZF=1, PC←PC+2	-	-	2	2	6A:ml	100
	JC	ml	jump if carry	if CF=1, PCmm, PCll if CF=0, PC←PC+2	-	-	2	2	6F:ml	101
	JNC	ml	jump if non-carry	if CF=0, PCmm, PCll if CF=1, PC←PC+2	-	-	2	2	6B:ml	101
	JBZ	bp, ml	jump if bit zero	if A(bp)=0, PCmm, PCll if A(bp)=1, PC←PC+2	-	-	2	2	7(8+bp):ml	102
	JBNZ	bp, ml	jump if bit nonzero	if A(bp)=1, PCmm, PCll if A(bp)=0, PC←PC+2	-	-	2	2	7(C+bp):ml	102
	CYIJ	n, ml	compare Y and jump	if Y≠n, PCmm, PCll if Y=n, PC←PC+2	-	●	2	2	Bn:ml	103
	NOP		no operation	PC←PC+1	-	-	1	1	00	103
I/O instructions	IN	p, n	input	A←PORT(p)&n	-	-	2	2	73:pn	104
	OUT	p, n	output	PORT(p)←A & n	-	-	2	2	72:pn	104
	ROUT	p, n	reset output	PORT(p)←PORT(p) & $\overline{n}$	-	-	2	2	62:pn	105
	SOUT	p, n	set output	PORT(p)←PORT(p) | n	-	-	2	2	66:pn	105
Control instructions	WI		wait for interrupt	SP←SP-4, M(SP)←PC+1	-	-	1	1	4A	106
	RC		reset carry	CF←0	0	-	1	1	03	107
	SC		set carry	CF←1	1	-	1	1	07	107
	EDI	m, n	enable/disable interrupt	IE←IE & $\overline{m}$ | n	-	-	2	2	5B:mn	108
	UPX0		up to X0	RAM_BANK_FF←0	-	-	1	1	51	111
	UPX1		up to X1	RAM_BANK_FF←1	-	-	1	1	50	111
	LUX		load UPX	A←RAM_BANK_FF	-	-	1	1	52	112

Note : "Page" refers to the corresponding page in the Instruction Manual.

10-3 Instruction Map

MN15G SERIES INSTRUCTION MAP



10-4 Differences between MN1500 and MN15G

Table 10-4-1 Differences between MN1500 (bank vers., linear vers.) And MN15G

	MN1500 series (bank vers., linear vers.)		MN15G series	
Instruction	WTSB	serial interface function is operated	WTSB	Data in units of 8-bits is written to the special buffer (SB).
	RDSB		RDSB	Data in units of 8-bits is read from the special buffer (SB).
	SBTIN		SBTIN	-
	SBTEX		SBTEX	-
	WTTC	timer function is operated	WTTC	-
	WTTB		WTTB	Data in units of 8-bits is written to the temporary buffer (TB).
	RDBC		RDBC	Data in units of 8-bits is read from the temporary buffer (TB).
Interrupt factor	External interrupt		Interrupt 1	
	Timer interrupt		Interrupt 2	
	Serial interrupt		Interrupt 3	

10-5 Special Function Registers List

MN15G0202 Special Function Registers List (1/2)

Address	Register	Bit Symbol								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
x'000'	PORT01	P13DATA	P12DATA	P11DATA	P10DATA	P03DATA	P02DATA	P01DATA	P00DATA	III - 9
		Port 1 I/O Data				Port 0 I/O Data				
x'002'	PORT23		P32DATA	P31DATA	P30DATA	P23DATA	P22DATA	P21DATA	P20DATA	III - 13
			Port 3 I/O Data			Port 2 I/O Data				
x'010'	P01DIR	P1DIR3	P1DIR2	P1DIR1	P1DIR0	P0DIR3	P0DIR2	P0DIR1	P0DIR0	III - 9
		Port 1 Direction Control				Port 0 Direction Control				
x'012'	P23DIR		P3DIR2	P3DIR1	P3DIR0	P2DIR3	P2DIR2	P2DIR1	P2DIR0	III - 13
			Port 3 Direction Control			Port 2 Direction Control				
x'022'	P23PLU		P3PLU2	P3PLU1	P3PLU0	P2PLU3	P2PLU2	P2PLU1	P2PLU0	III - 13
			Port 3 Pull-up Control			Port 2 Pull-up Control				
x'028'	P01SC	P1SC3	P1SC2	P1SC1	P1SC0					III - 9
		Port 1 Output Structure Control								
x'02A'	P23SC		P3SC2	P3SC1	P3SC0	P2SC3	P2SC2	P2SC1	P2SC0	III - 14
			Port 3 Output Structure Control			Port 2 Output Structure Control				
x'030'	CPUM							CLKSEL1		II - 15
								System clock division switching		
x'032'	IRQM	IFIRQ3E	IFIRQ2E	IFIRQ1E						IV - 16
		Clear IRQ3 flag	Clear IRQ2 flag	Clear IRQ1 flag						
x'034'	IRQC0	MASKIR1	IRQ1SE0	reserved	reserved					IV - 16
		IRQ1 interrupt edge mask	IRQ1interrupt edge switching	Set to "0".	Set to "0".					
x'036'	IRQC1					MASKIR3	IRQ3SE	IRQ3S1	IRQ3S0	IV - 17
						IRQ3 interrupt mask	IRQ3 interrupt edge switching	IRQ3 interrupt source		
x'038'	KEYCNT		KEY2EN	KEY1EN	KEY0EN					IV - 17
			Enable Key interrupt (key0 to key2)							
x'03A'	ACZCNT						NSYNCS	ACZ1IN	reserved	VII - 5
							P30 output data switching	P31 input data switching	Set to "0".	
x'044'	TM2BC	TM2BC7	TM2BC6	TM2BC5	TM2BC4	TM2BC3	TM2BC2	TM2BC1	TM2BC0	V - 10
		Timer 2 binary counter								
x'046'	TM3BC	TM3BC7	TM3BC6	TM3BC5	TM3BC4	TM3BC3	TM3BC2	TM3BC1	TM3BC0	V - 10
		Timer 3 binary counter								
x'04C'	TM2MD				TM2PWM	TM2EN	TM2CK2	TM2CK1	TM2CK0	V - 11
					Timer 2 PWM Selection	Timer 2 count enable	Timer 2 count clock			
X'04E'	TM3MD				TM3CAS	TM3EN	TM3CK2	TM3CK1	TM3CK0	V - 12
					Timer 2 & Timer 3 Cascade connection	Timer 3 count enable	Timer 3 count clock			

MN15G0202 Special Function Registers List (2/2)

Address	Register	Bit Symbol								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
x'054'	TM2OC	TM2OC7	TM2OC6	TM2OC5	TM2OC4	TM2OC3	TM2OC2	TM2OC1	TM2OC0	V - 9
		Timer 2 Compare Register								
x'056'	TM3OC	TM3OC7	TM3OC6	TM3OC5	TM3OC4	TM3OC3	TM3OC2	TM3OC1	TM3OC0	V - 9
		Timer 3 Compare Register								
x'05E'	MODCNT						PWMOS0			V - 12
							Timer Output Selection			
x'06A'	TCOCNT	TCOE	RMOEN	RMDTY		RMOS	TCOS	TC23OS		V - 13
		Timer Output Enable	Remote Control Output Enable	Remote Control Output Duty Selection		TCO output Selection	Timer, Buzzer Output Selection	Timer 2, Timer 3 Output Selection		
x'06C'	BZCTR			BZCK1	BZCK0	PWME13	PWME12	PWME11	PWME10	V - 14
				Buzzer Output Frequency Selection		Port 13 PWM Output Enable	Port 12 PWM Output Enable	Port 11 PWM Output Enable	Port 10 PWM Output Enable	
x'06E'	WDCTR								WDTCLR	VIII - 4
									Clear Watchdog Timer	
x'070'	ADBUF0	ADBUF1	ADBUF0							VI - 6
		A/D Conversion Data Storage Buffer 1-0								
x'072'	ADBUF1	ADBUF9	ADBUF8	ADBUF7	ADBUF6	ADBUF5	ADBUF4	ADBUF3	ADBUF2	VI - 6
		A/D Conversion Data Storage Buffer 9-2								
x'074'	ADCTR0	ADST	ADSH1	ADSH0	ADCK	ADLADE		ADCHS1	ADCHS0	VI - 5
		A/D Conversion Status	Sample and Hold Time Setup		A/D Conversion Clock Selection	A/D Ladder Resistance Selection		A/D Conversion Input Selection		

10-6 Circuit Setup

10-6-1 General Usage

■Connection of V_{DD} pin, and V_{SS} pin

All of the V_{DD} and V_{SS} pins are external. Connect them directly to the power source and ground. Put them on printed circuit board after the location of LSI (package) pin is considered.
Incorrect connection may lead a fusion and break a microcontroller.

■Cautions for Operation

(1) If you install the product close to high-field emissions (under the cathode ray tube), shield the package surface to ensure normal performance.

(2) Operation temperature should be well considered. Each product has different condition. For example, if the operation temperature is over the condition, its operation may be executed wrongly.

(3) Operation voltage should be also well considered. Each product has different operating range.
- If the operation voltage is over the operating range, the length of its life may be shortened .
- If the operation voltage is below the operating range, it operation may be executed wrongly.

10-6-2 Unused Pins

■Unused Functions

Unused functions should be set as operation is off.

■Port 3

Port 3 is input pin in the initial status. So if the input is unstable, both of the Pch transistor and Nch transistor of the input inverter are operated so that the through current is happened and the electricity consumption is wasted, the power inside of chip can be damaged by noise. Pull-up or pull-down should be added, when they are not used.

Note : The above is in the case of the initial status (input). If the pin's direction is switched to output, set them open.

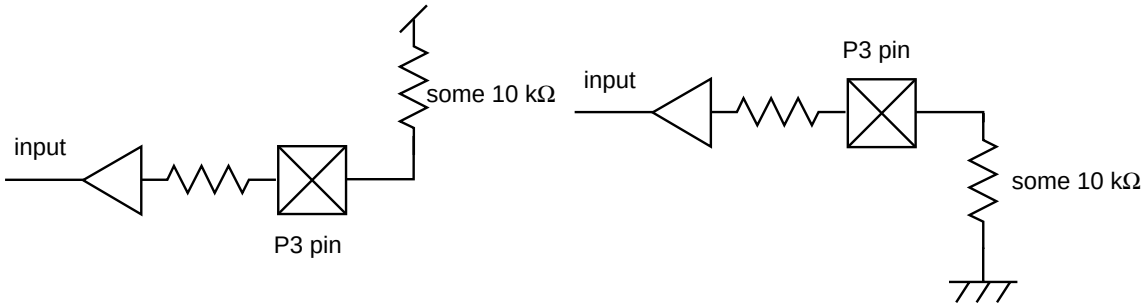


Figure 10-6-1 Port 3 (input)

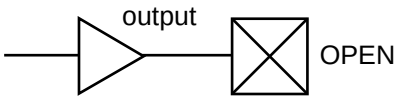


Figure 10-6-2 Port 3 (output)

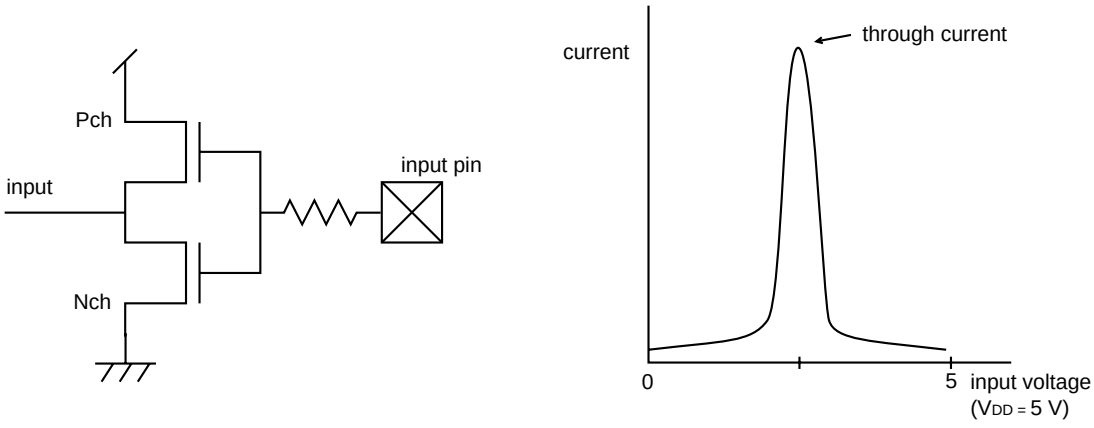


Figure 10-6-3 Input Inverter Organization and Characteristics

■Port 0, port 1, port 2

The initial status of port 1, port 2 and port 3 is input pin, but gate is opened only at the execution of input instruction so that the through current cannot be happened. As they are not used, they should be open nevertheless of pin's direction.

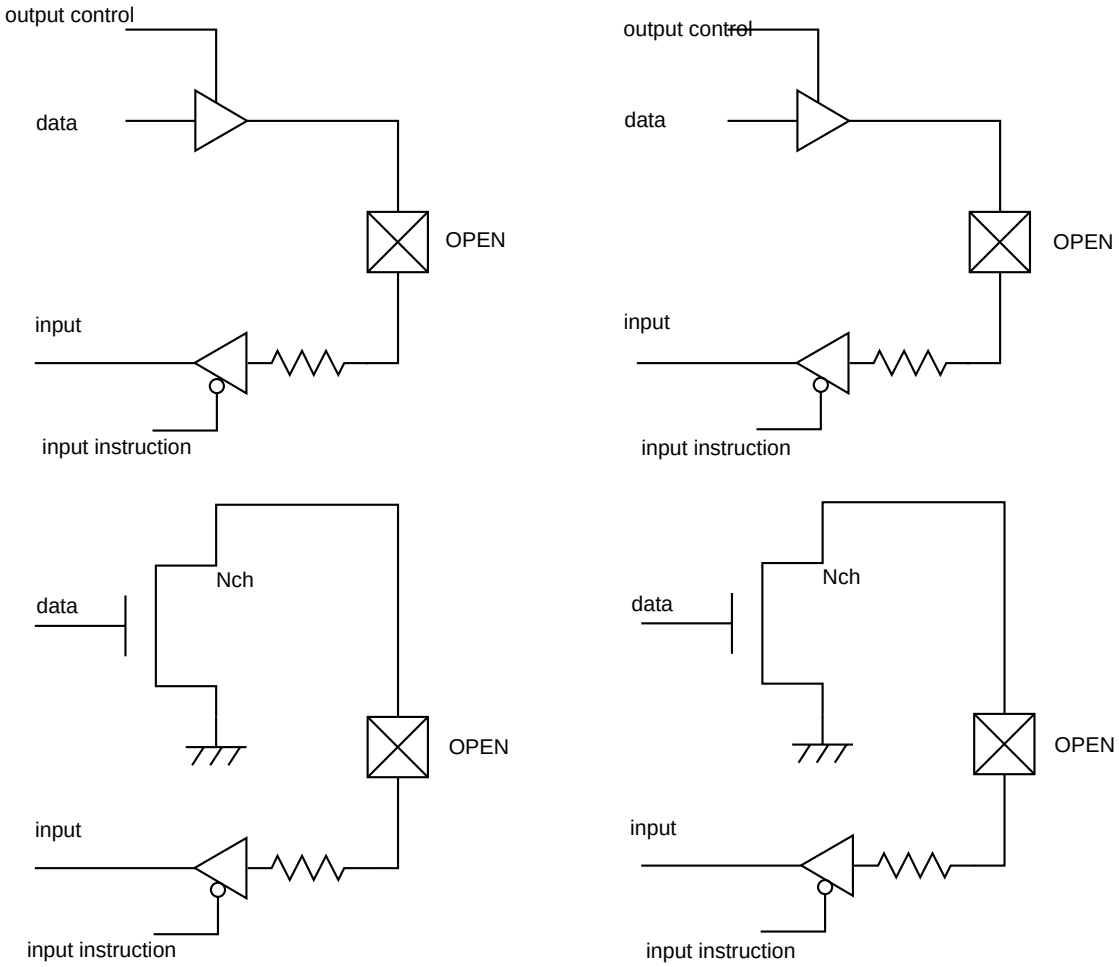


Figure 10-6-4 Port 0, Port 1, Port 2

10-6-3 Power Supply

■The Relation between Power Supply and Input Pin Voltage

Input pin voltage should be supplied only after power supply is on. If the input voltage is supplied before Vdd is on, a latch up occurs and causes the destruction of micro controller by a large current flow.

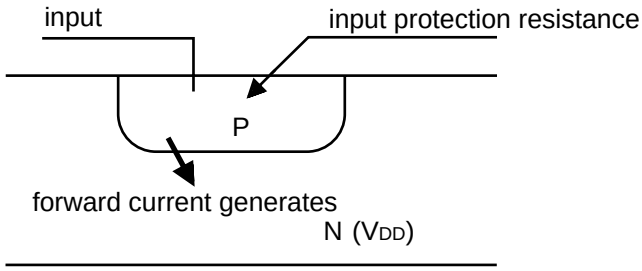


Figure 10-6-5 V_{DD} and Input Pin Voltage

■The Relation between V_{DD} and Reset Input Voltage

After power supply is on, reset pin voltage should be low for sufficient time before rising , in order to be recognized as a reset signal.

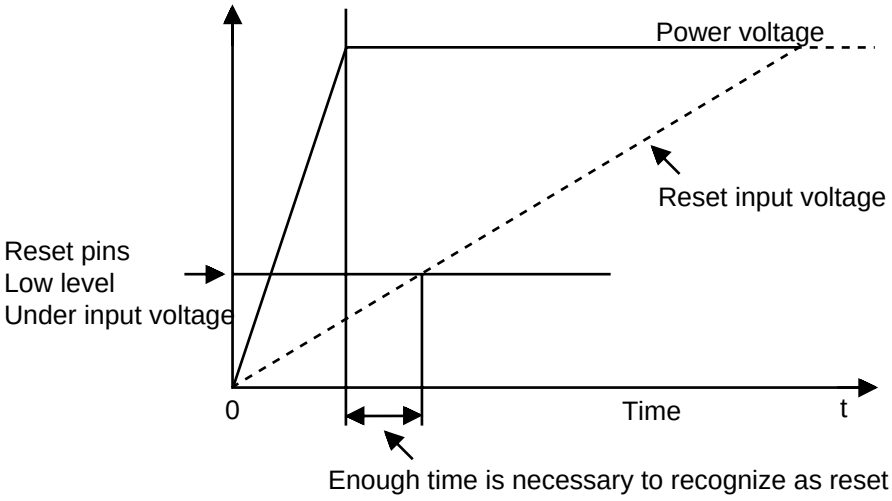


Figure 10-6-6 Power Supply and Reset Input Voltage

10-6-4 Power Supply Circuit

■Cautions for Setting Power Supply Circuit

The CMOS logic microcontroller is high speed and high density. So, the power circuit should be designed, taking into consideration of AC line noise, ripple caused by LED driver. Figure 10-6-7 shows an example for emitter follower type power supply circuit.

■An Example for a Circuit of V_{DD} Supply (Emitter follower type)

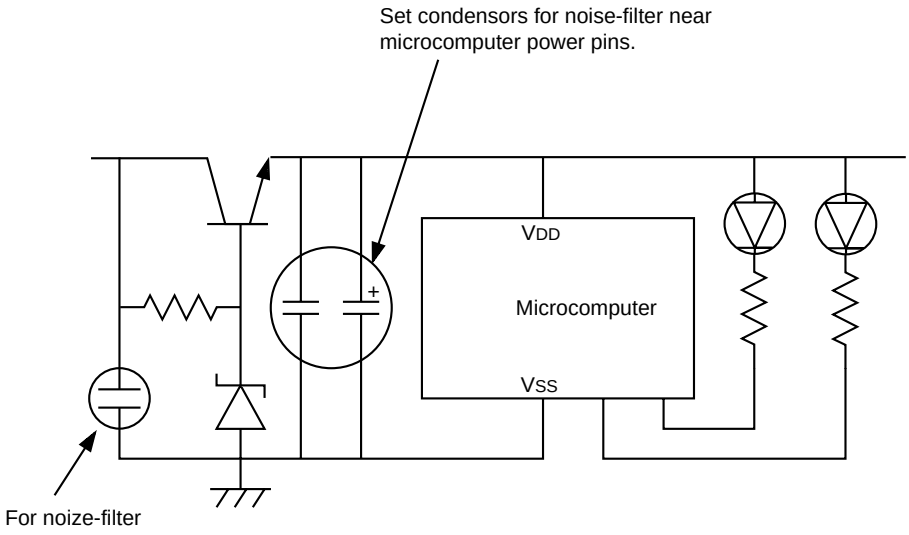


Figure 10-6-7 An Example for a Circuit of V_{DD} Supply (Emitter follower type)

Record of Changes

MN15G0202/0402 LSI User's Manual Record of Changes (First Edition to Second Edition) (1/3)

Page	Definition	Details of Changes	
		Previous Edition (First Edition)	New Edition (Second Edition)
-	Change	(Product name) MN15GP0402	MN15GP0402SJ
I - 2	Delete	[Table 1-1-2. Differences in Models]	Mask Option: Oscillation circuit
I - 3	Delete	Machine Cycle When automatic reset is not used When automatic reset circuit 1 is used When automatic reset circuit 2 is used	122µs / 32.768 kHz divided by 4 (2.0 V to 5.5 V)
I - 4	Delete	Mask Option	(Oscillation is selected from high / low / RC.)
		Port	- NRST input 1 ports
	Addition		- Key input 3 ports (for NSYNC output, NIRQ input, ACZ input, timer output and buzzer output, too) - PWM output 4 ports
I - 5	Delete	[Table 1-3-1. Functions on Blocks] Clock generator: Clock generator Block: Connect resonator to OSC1,OSC2 to generate system clock. At RC oscillation in mask option, connect RC to external to generate system clock.	Underlined part is deleted.
I - 8	Delete	[Table 1-4-1. Pin Function Summary (1/3)] OSC1, OSC2: Connect these oscillation pins to oscillators for clock operation. Feedback resistor is built-in. (Not connected at RC oscillation)	Underlined part is deleted.
		NRST: After reset is cleared,internal reset is cleared after 2^{14} counts of OSC input clock at high oscillation, and 27 counts of OSC input clock at low/RC oscillation.	Underlined part is deleted.
I - 14 to I - 18	Change	[Chapter 1-4-1. Operating Conditions]	Specifications, figures and warnings on low oscillation and RC oscillation are deleted. Tables relevant to deletion in the specification are changed.

MN15G0202/0402 LSI User's Manual Record of Changes (First Edition to Second Edition) (2/3)

Page	Definition	Details of Changes	
		Previous Edition (First Edition)	New Edition (Second Edition)
I - 19	Delete	[Chapter 1-6-3. DC Characteristics]	Specifications and warnings on low oscillation and RC oscillation are deleted. Tables relevanat to deletion in the specification are changed.
	Addition		- During STOP mode, The supply current IDD4, IDD5 and IDD6 are applied to the circuit other than the auto reset circuit.
I - 24	Change	[Chapter 1-7. External Dimensions] Package code : *SOP020-P-0300	Package code : * SOP020-P-0300D
	Addition		Warnings
I - 25	Delete	[Chapter 1-8-1. Mask Option]	1. Oscillation circuit setup
I - 26	Change	[Chapter 1-8-2. Option Check List Ver.0.04)]	[Chapter 1-8-2. Option Check List Ver.0.05)]
	Delete	3. Automatic reset circuit V_{RSTL2} cannot be selected at RC oscillation, and at tc (the instruction execution time) < 2 µs.	2. OSC oscillation circuit is deleted Underlined part is deleted
II - 2	Delete	[Chapter 2-1-1. Clock Generator] OSC oscillation can be selected from high speed / low speed / RC by mask option. When high speed oscillation or low speed oscillation is selected, these circuits require external oscillators and capacitors. Connect a crystal or ceramic oscillator (Figure 2-1-1(a)). When RC oscillation is selected, the circuit require external capacitors and resistors. Oscillation frequency may be changed by capacitors, resistors, temperature and voltage or so (Figure 2-1-1(b)).	Underlined part is deleted. Oscillator circuit connection (b) is deleted.
II - 3	Delete	[Chapter 2-1-2. CPU Basic Timing] At 4.0MHz, at high speed oscillation, 1 machine cycle is 1.0 µs at divided by 4, and 2.0 µs at divided by 8. At 32 kHz at low speed oscillation, 1 machine cycle is 122 µs at divided by 4, 250 µs at divided by 8.	Underlined part is deleted.
II - 14	Delete	[Chapter 2-4-1. Clock Switching] At fosc=4.0 MHz, instruction cycle is 1.0 µs at divided by 4, and 2.0 µs at divided by 8. And at fosc=32 kHz, 125 µs at divided by 4.	Underlined part is deleted.

MN15G0202/0402 LSI User's Manual Record of Changes (First Edition to Second Edition) (3/3)

Page	Definition	Details of Changes	
		Previous Edition (First Edition)	New Edition (Second Edition)
II - 20	Delete	[■Timing of reset release] After the NRST pin becomes "H", there is 2^{14} pulse counts of OSC input clock (fosc) at high speed oscillation, 2^{7} pulse counts at low speed oscillation, RC oscillation till the internal reset is released.	Underlined part is deleted.
V - 23	Change	[■PWM Output Setup Example (Timer 2)] The 1/4 duty cycle PWM output waveform is output from the TCO output pin at 128 Hz by using timer 2.	The 1/4 duty cycle PWM output waveform is output from the TCO output pin at 244 Hz by using timer 2.
	Change	The oscillation is at low frequency oscillation (fx), at fosc = 32.768 kHz.	The oscillation is fosc = 4 MHz.
	Change	[Setup procedure] (4) Select the count clock source. TM2MD (x'04C') bp2-0:TM2CK2-0= 100 [Discription] (4) Select fosc as clock source by the TM2CK2-0 flag of the TM2MD register.	[Setup procedure] (4) Select the count clock source. TM2MD (x'04C') bp2-0:TM2CK2-0= 111 [Discription] (4) Select fosc/64 as clock source by the TM2CK2-0 flag of the TM2MD register.
IX - 3	Change	[Table 9-1-2. Electrical Characteristics]	
X - 2	Delete	These include the MN15G0202, MN15G0402 variants MN15GP0402SJ and PX-AP15G0402-SY. The PX-AP15G0402 is sealed in a ceramic package with a window. Written data can be erased by exposing the physical chip to intense ultraviolet radiation. - Erasing Data in Windowed Package (PX-AP15G0402-SY)	Underlined parts are deleted.
	Change	Warning: PX-AP 15G0402-SY is not available for engineering sample now.	Warning: The PX-AP15G0402-SY with windowed ceramic package is not supplied.
X - 3	Delete	[Chapter 10-1-2 Cautions on Use]	Discription (1) is deleted.
X - 4	Delete	[Chapter 10-1-3. Erasing Data in Windowed Package (PX-AP15G0402-SY)]	
X - 5	Delete	[Chapter 10-1-4. Differences between Mask ROM version and EPROM version]	Mask option: Oscillation circuit

MN15G0202/0402
LSI User's Manual

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